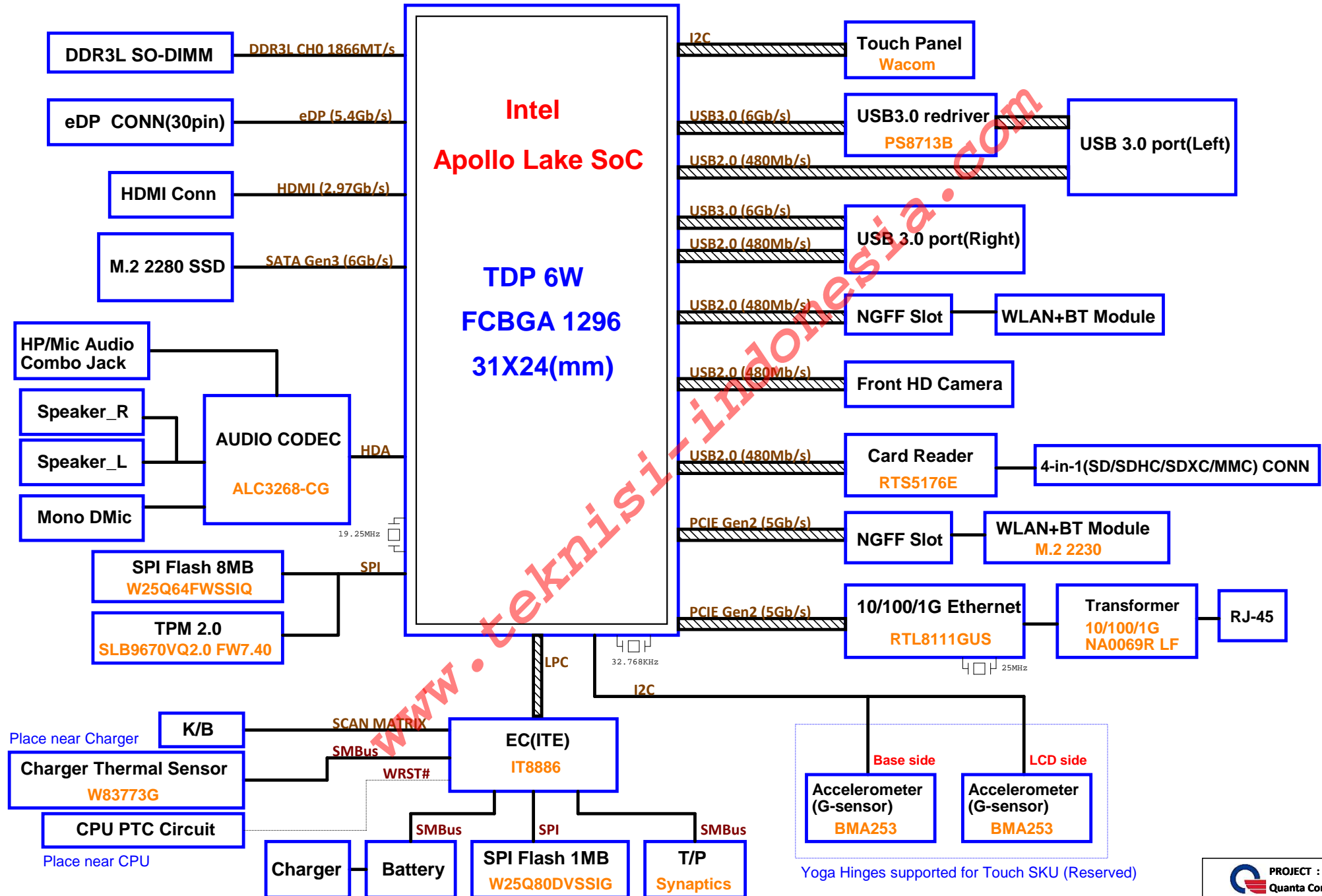
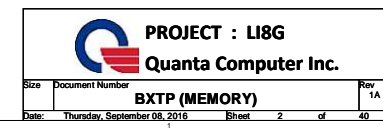
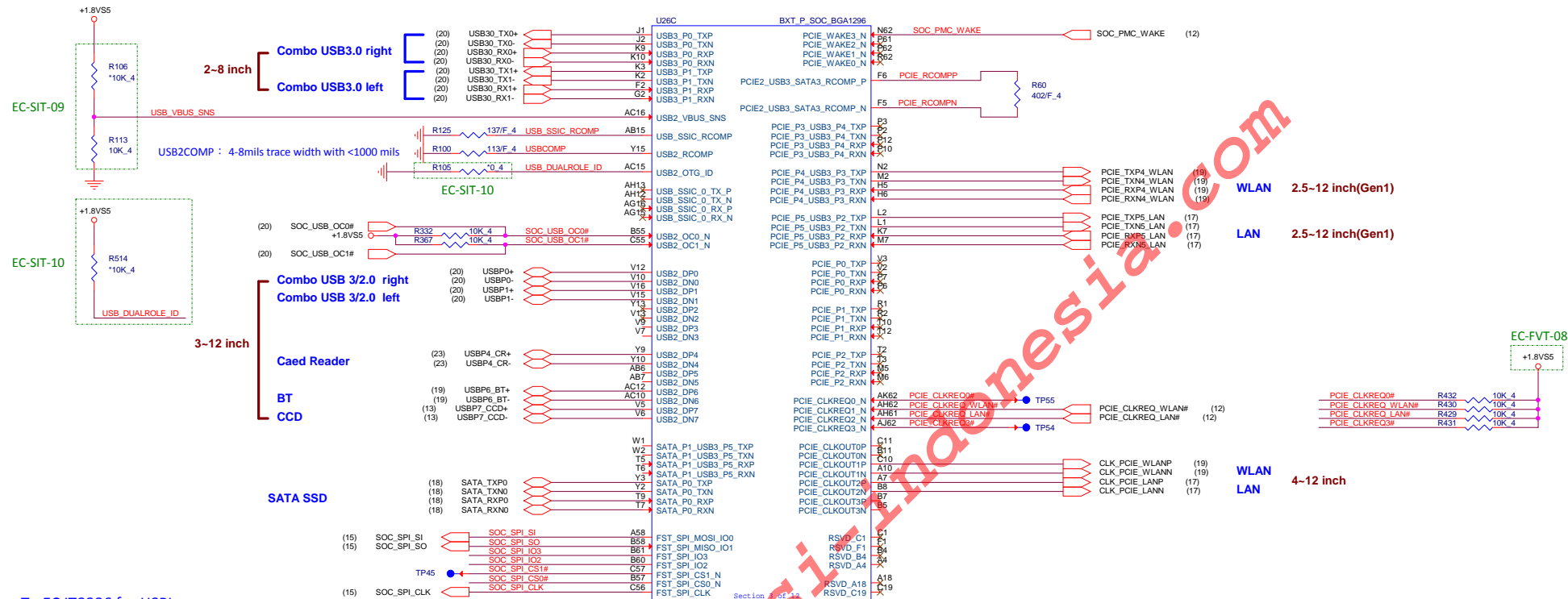


Newton II Intel APL Platform UMA Block Diagram (Windows)

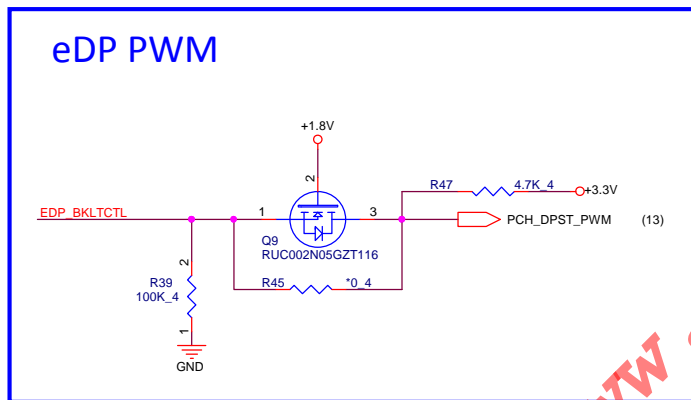
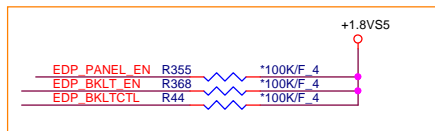


+1.35VSUS 

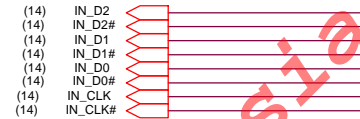




SPI ROM	Vender	Size	Quanta P/N	Vender P/N
1.8V	WND	8MB	AKE5EZN0N01	W25Q64FWSSIQ

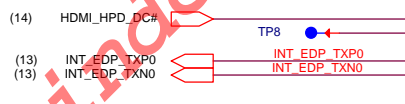


Max 7.5 inch HDMI



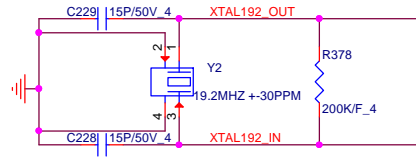
DDI0_HPD

DDI1_HPD

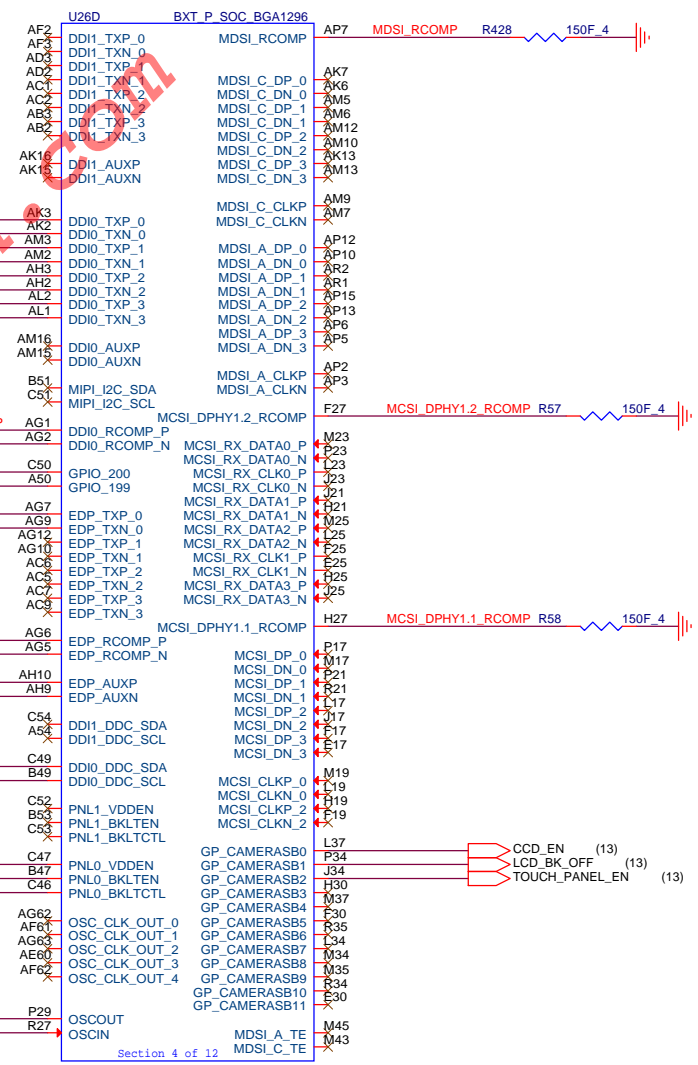


eDP Panel

<10000 mil



<1000 mil



PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	BXTP (HDMI/eDP)	1A
Date:	Thursday, September 08, 2016	Sheet 4 of 40

Refer to EDS, need change to Function 3 for pin H52

use for SPI TPM chip select

(15) SOC_SPI_CS2#_TPM SOC_SPI_CS2#_TPM

Pull low for normal platform operation

Pull low for normal platform operation

LPC 1.8V/3.3V mode select

Boot BIOS Strap

Pull low for normal platform operation

Pull low for normal platform operation

Pull low for normal platform operation

Top swap override

Pull low for normal platform operation

Pull high for normal platform operation

LPC set 3.3V

Enable CSE(TXE3.0) ROM Bypass

RTC Clock Timer Bypass

Allow eMMC as a boot source

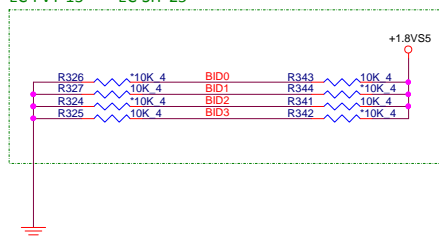
Allow SPI as a boot source

Force DNX FW Load

Pull low for normal platform operation

BOARD ID SETTING

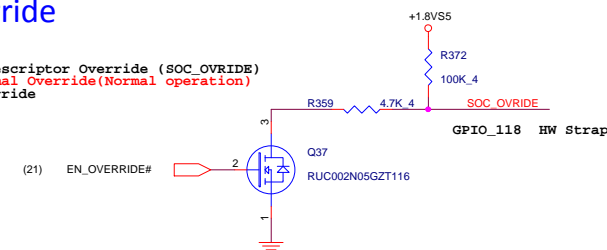
EC-FVT-13 EC-SIT-25



SKU	BID_0	BID_1	BID_2	BID_3
SDV Non-Touch	0	0	0	0
SDV Touch	1	0	0	0
FVT Non-Touch	0	0	0	1
FVT Touch	1	0	0	1
SIT Non-Touch	0	0	1	0
SIT Touch	1	0	1	0
SVT Non-Touch				
SVT Touch				

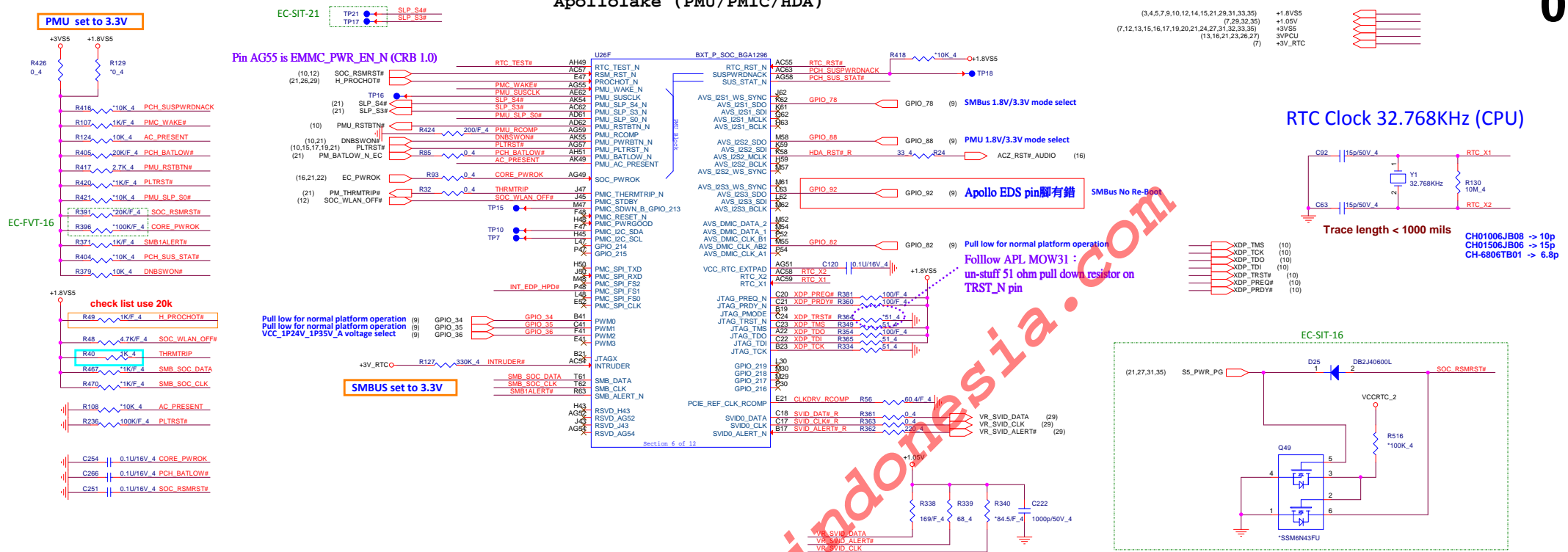
Override

Flash Descriptor Override (SOC_OVERRIDE)
0 = Normal Override(Normal operation)
1 = Override

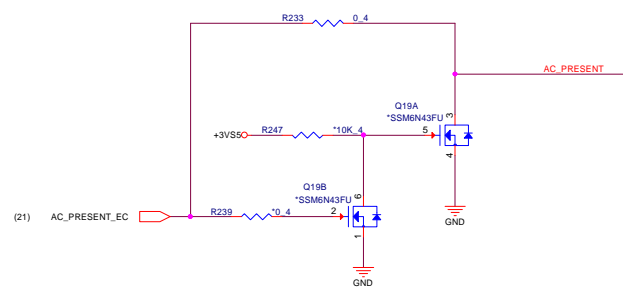


PROJECT : LI8G
Quanta Computer Inc.

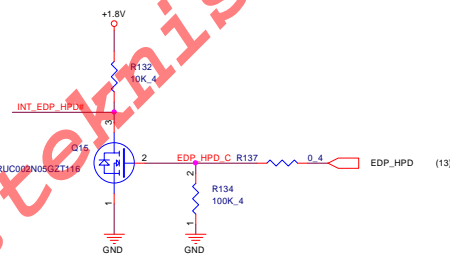
Size Document Number
BXTB (GPIO/LPC/I2C/HDA)
Date: Friday, September 09, 2016 Sheet 5 of 40



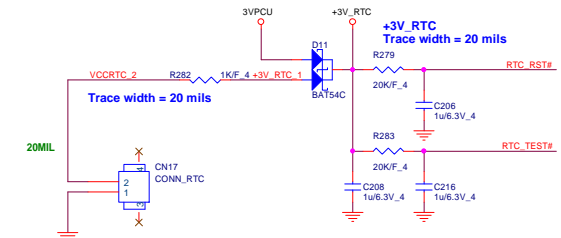
AC_PRESENT



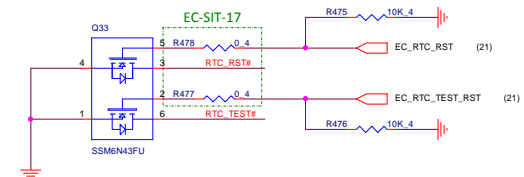
eDP HPD



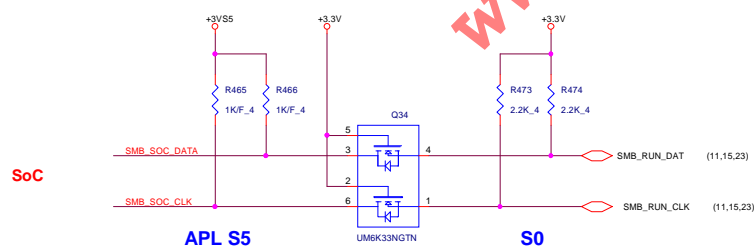
RTC Circuitry (RTC)



EC reset RTC



SMBus



DDR3L
Click Pad

+VNN Output Decoupling Recommendations			
1uFx3	0402	BOT, inside socket cavity	
22uFx4	0603	TOP, inside socket cavity	

VDD2_1P24_GLM_L Output Decoupling Recommendations			
1uFx3	0402	TOP*1 / BOT*3, inside socket cavity	
22uFx1	0603	TOP, inside socket cavity	

VDD2_1P24_DSI_CSI Output Decoupling Recommendations			
1uFx2	0402	TOP*1 / BOT*1, inside socket cavity	
22uFx1	0603	TOP, inside socket cavity	

VDD2_1P24_AUD_ISH_PLL Output Decoupling Recommendations			
1uFx2	0402	TOP*1 / BOT*1, inside socket cavity	
22uFx1	0603	TOP, inside socket cavity	

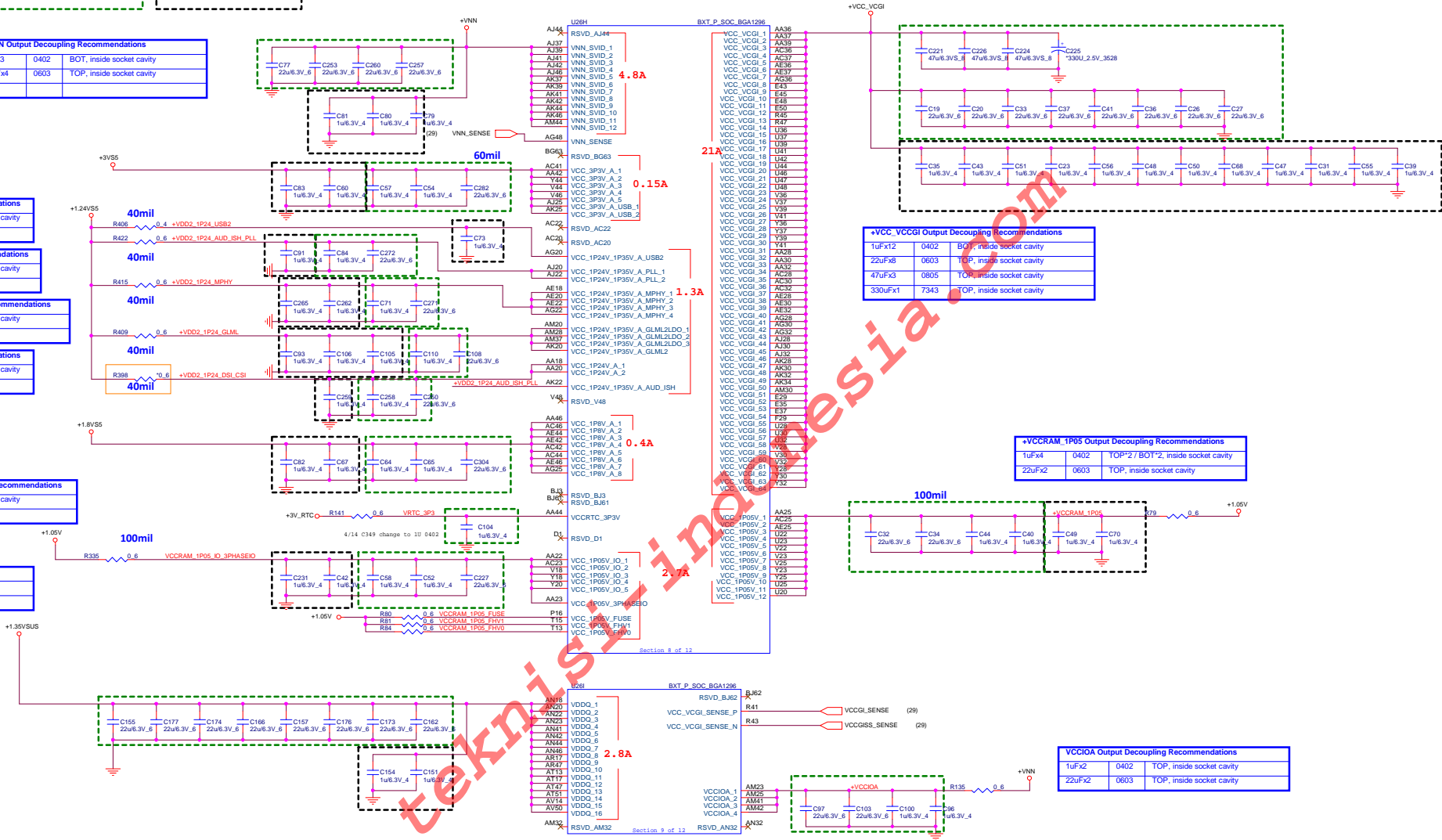
VDD2_1P24_MPHY Output Decoupling Recommendations			
1uFx3	0402	TOP*1 / BOT*2, inside socket cavity	
22uFx1	0603	TOP, inside socket cavity	

VCCRAM_1P05_IO_3PHASEIO Output Decoupling Recommendations			
1uFx4	0402	TOP*2 / BOT*2, inside socket cavity	
22uFx1	0603	TOP, inside socket cavity	

+VCCDDQ Output Decoupling Recommendations			
1uFx2	0402	BOT, inside socket cavity	
22uFx8	0603	TOP, inside socket cavity	

+VCCRAM_1P05 Output Decoupling Recommendations			
1uFx4	0402	TOP*2 / BOT*2, inside socket cavity	
22uFx2	0603	TOP, inside socket cavity	

VCCIOA Output Decoupling Recommendations			
1uFx2	0402	TOP, inside socket cavity	
22uFx2	0603	TOP, inside socket cavity	



Apollolake ULT (GND)

08

U26J BXT_P_SOC_BGA1296			
R29	VSS_1	VSS_82	AH58
A12	VSS_2	VSS_83	AH59
A16	VSS_3	VSS_84	AH6
A20	VSS_4	VSS_85	AH7
A24	VSS_5	VSS_86	AJ1
A28	VSS_6	VSS_87	AJ18
A32	VSS_7	VSS_88	AJ2
A36	VSS_8	VSS_89	AJ23
A40	VSS_9	VSS_90	AJ27
A44	VSS_10	VSS_91	AJ34
A48	VSS_11	VSS_92	AJ36
A5	VSS_12	VSS_93	AJ63
A52	VSS_13	VSS_94	AK10
A56	VSS_14	VSS_95	AK12
A62	VSS_15	VSS_96	AK18
A9	VSS_16	VSS_97	AK23
AA1	VSS_17	VSS_98	AK27
AA2	VSS_18	VSS_99	AK36
AA27	VSS_19	VSS_100	AK48
AA34	VSS_20	VSS_101	AK5
AA41	VSS_21	VSS_102	AK52
AA63	VSS_22	VSS_103	AK59
AB10	VSS_23	VSS_104	AK9
AB12	VSS_24	VSS_105	AM18
AB16	VSS_25	VSS_106	AM22
AB48	VSS_26	VSS_107	AM27
AB5	VSS_27	VSS_108	AM34
AB52	VSS_28	VSS_109	AM36
AB57	VSS_29	VSS_110	AM39
AB59	VSS_30	VSS_111	AM46
AB9	VSS_31	VSS_112	AN1
AC18	VSS_32	VSS_113	AN10
AC27	VSS_33	VSS_114	AN11
AC34	VSS_34	VSS_115	AN13
AC39	VSS_35	VSS_116	AN14
AE1	VSS_36	VSS_117	AN16
AE10	VSS_37	VSS_118	AN17
AE11	VSS_38	VSS_119	AN2
AE13	VSS_39	VSS_120	AN25
AE14	VSS_40	VSS_121	AN27
AE16	VSS_41	VSS_122	AN28
AE17	VSS_42	VSS_123	AN30
AE2	VSS_43	VSS_124	AN34
AE23	VSS_44	VSS_125	AN36
AE27	VSS_45	VSS_126	AN37
AE34	VSS_46	VSS_127	AN39
AE39	VSS_47	VSS_128	AN47
AE4	VSS_48	VSS_129	AN48
AE41	VSS_49	VSS_130	AN5
AE47	VSS_50	VSS_131	AN50
AE48	VSS_51	VSS_132	AN51
AE5	VSS_52	VSS_133	AN53
AE50	VSS_53	VSS_134	AN54
AE51	VSS_54	VSS_135	AN56
AE53	VSS_55	VSS_136	AN57
AE54	VSS_56	VSS_137	AN59
AE56	VSS_57	VSS_138	AN63
AE57	VSS_58	VSS_139	AN7
AE59	VSS_59	VSS_140	AN8
AE63	VSS_60	VSS_141	AP55
AE7	VSS_61	VSS_142	AP9
AE8	VSS_62	VSS_143	AR19
AG13	VSS_63	VSS_144	AR32
AG18	VSS_64	VSS_145	AR45
AG23	VSS_65	VSS_146	AT12
AG27	VSS_66	VSS_147	AT16
AG34	VSS_67	VSS_148	AT19
AG37	VSS_68	VSS_149	AT2
AG39	VSS_69	VSS_150	AT25
AG41	VSS_70	VSS_151	AT29
AG42	VSS_71	VSS_152	AT3
AG44	VSS_72	VSS_153	AT35
AG46	VSS_73	VSS_154	AT39
AH15	VSS_74	VSS_155	AT45
AH16	VSS_75	VSS_156	AT48
AH48	VSS_76	VSS_157	AT52
AH5	VSS_77	VSS_158	AT57
AH52	VSS_78	VSS_159	AT61
AH54	VSS_79	VSS_160	AT62
AH55	VSS_80	VSS_161	AT7
AH57	VSS_81	VSS_162	AU32

Section 10 of 12

U26K BXT_P_SOC_BGA1296			
AV19	VSS_163	VSS_244	BG29
AV2	VSS_164	VSS_245	BG32
AV21	VSS_165	VSS_246	BG35
AV23	VSS_166	VSS_247	BG41
AV29	VSS_167	VSS_248	BG45
AV3	VSS_168	VSS_249	BH1
AV32	VSS_169	VSS_250	BH2
AV35	VSS_170	VSS_251	BH21
AV41	VSS_171	VSS_252	BH25
AV43	VSS_172	VSS_253	BH39
AV45	VSS_173	VSS_254	BH43
AV55	VSS_174	VSS_255	BH43
AV61	VSS_175	VSS_256	BH62
AV62	VSS_176	VSS_257	BH63
AV9	VSS_177	VSS_258	BJ10
AW14	VSS_178	VSS_259	BJ14
AW30	VSS_179	VSS_260	BJ18
AW34	VSS_180	VSS_261	BJ28
AW50	VSS_181	VSS_262	BJ32
AY10	VSS_182	VSS_263	BJ36
AY32	VSS_183	VSS_264	BJ4
AY54	VSS_184	VSS_265	BJ46
AY58	VSS_185	VSS_266	BJ50
AY6	VSS_186	VSS_267	BJ54
B2	VSS_187	VSS_268	BJ56
B3	VSS_188	VSS_269	BJ60
B62	VSS_189	VSS_270	C12
B63	VSS_190	VSS_271	C16
B9	VSS_191	VSS_272	C28
BA1	VSS_192	VSS_273	C32
BA12	VSS_193	VSS_274	C40
BA16	VSS_194	VSS_275	C48
BA17	VSS_195	VSS_276	D32
BA2	VSS_196	VSS_277	D58
BA21	VSS_197	VSS_278	D6
BA25	VSS_198	VSS_279	E12
BA27	VSS_199	VSS_280	E14
BA29	VSS_200	VSS_281	E19
BA32	VSS_201	VSS_282	E27
BA35	VSS_202	VSS_283	E4
BA37	VSS_203	VSS_284	E54
BA39	VSS_204	VSS_285	F10
BA43	VSS_205	VSS_286	F21
BA47	VSS_206	VSS_287	F3
BA48	VSS_207	VSS_288	F32
BA52	VSS_208	VSS_289	F37
BA62	VSS_209	VSS_290	F43
BA63	VSS_210	VSS_291	F45
BB19	VSS_211	VSS_292	F50
BB25	VSS_212	VSS_293	F56
BB3	VSS_213	VSS_294	F59
BB39	VSS_214	VSS_295	F63
BB45	VSS_215	VSS_296	G1
BB61	VSS_216	VSS_297	G32
BC32	VSS_217	VSS_298	H17
BD3	VSS_218	VSS_299	H23
BD32	VSS_219	VSS_300	H29
BD56	VSS_220	VSS_301	H3
BD61	VSS_221	VSS_302	H37
BD8	VSS_222	VSS_303	H47
BE1	VSS_223	VSS_304	H61
BE10	VSS_224	VSS_305	H7
BE12	VSS_225	VSS_306	J12
BE16	VSS_226	VSS_307	J14
BE17	VSS_227	VSS_308	J19
BE21	VSS_228	VSS_309	J27
BE27	VSS_229	VSS_310	J30
BE29	VSS_230	VSS_311	J32
BE35	VSS_231	VSS_312	J35
BE37	VSS_232	VSS_313	J37
BE43	VSS_233	VSS_314	J48
BE47	VSS_234	VSS_315	J63
BE48	VSS_235	VSS_316	K32
BE52	VSS_236	VSS_317	K5
BE54	VSS_237	VSS_318	K54
BE63	VSS_238	VSS_319	K57
BF3	VSS_239	VSS_320	K6
BF32	VSS_240	VSS_321	L21
BF61	VSS_241	VSS_322	L27
BG19	VSS_242	VSS_323	L29
BG23	VSS_243	VSS_324	L35

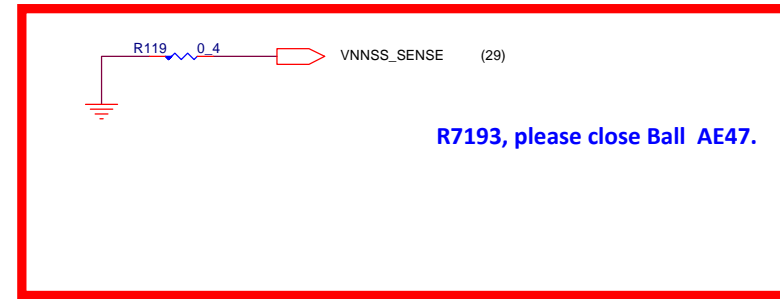
Section 11 of 12

U26L BXT_P_SOC_BGA1296			
L43	VSS_325	VSS_361	U2
L45	VSS_326	VSS_362	U27
L50	VSS_327	VSS_363	U34
M14	VSS_328	VSS_364	U5
M21	VSS_329	VSS_365	U50
M27	VSS_330	VSS_366	U51
M3	VSS_331	VSS_367	U53
M32	VSS_332	VSS_368	U54
M50	VSS_333	VSS_369	U56
M59	VSS_334	VSS_370	U57
M9	VSS_335	VSS_371	U59
N1	VSS_336	VSS_372	U62
N32	VSS_337	VSS_373	U63
N63	VSS_338	VSS_374	U7
P13	VSS_339	VSS_375	U8
P19	VSS_340	VSS_376	U20
P35	VSS_341	VSS_377	U27
P37	VSS_342	VSS_378	U34
P41	VSS_343	VSS_379	U42
P43	VSS_344	VSS_380	Y12
P45	VSS_345	VSS_381	Y16
P5	VSS_346	VSS_382	Y22
P55	VSS_347	VSS_383	Y27
P59	VSS_348	VSS_384	Y34
P9	VSS_349	VSS_385	Y42
R23	VSS_350	VSS_386	Y46
R32	VSS_351	VSS_387	Y48
T49	VSS_352	VSS_388	Y5
U1	VSS_353	VSS_389	Y52
U10	VSS_354	VSS_390	Y54
U11	VSS_355	VSS_391	Y55
U13	VSS_356	VSS_392	Y57
U14	VSS_357	VSS_393	Y59
U16	VSS_358	VSS_394	Y6
U17	VSS_359	VSS_395	Y7
U18	VSS_360		

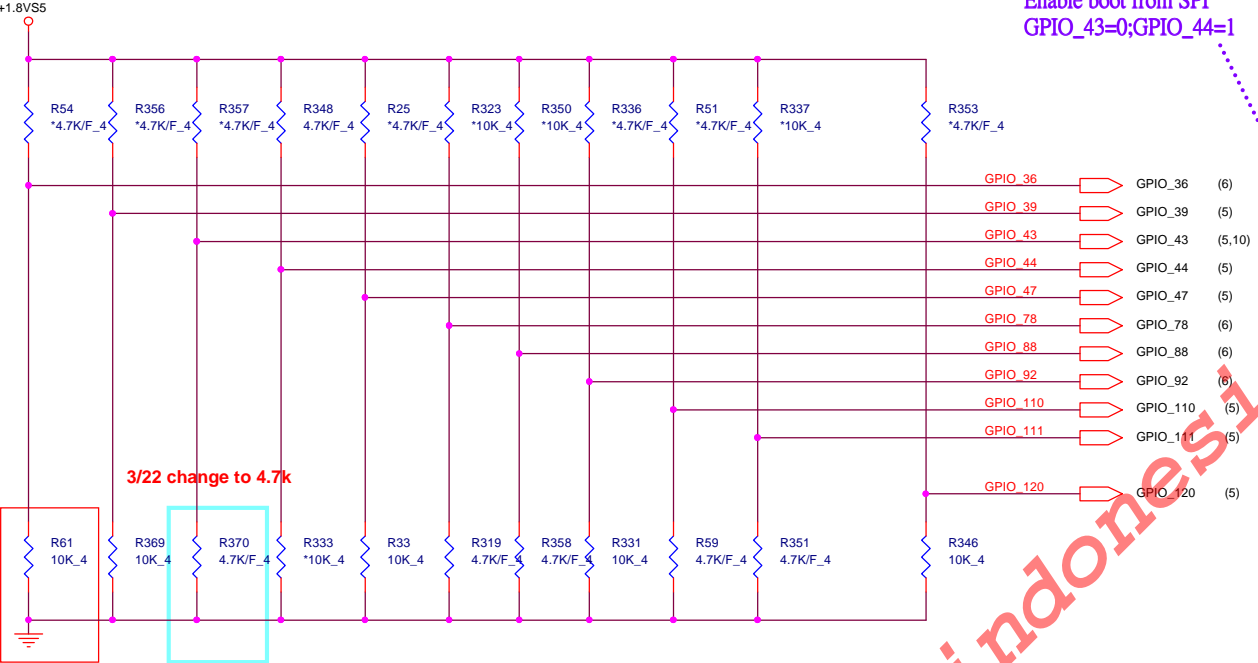
Section 12 of 12

U26G BXT_P_SOC_BGA1296			
B13	SPARE_9	NOCONNECT_16	M12
C13	SPARE_8	NOCONNECT_17	C15
L16	SPARE_7	NOCONNECT_18	F16
M16	SPARE_6	NOCONNECT_19	J16
E23	SPARE_5	NOCONNECT_20	D8
F23	SPARE_4	NOCONNECT_21	E8
R25	SPARE_3	NOCONNECT_22	H16
AB49	SPARE_2	NOCONNECT_23	C9
AC13	SPARE_11	NOCONNECT_24	F8
AB13	SPARE_10	NOCONNECT_25	E10
AM59	SPARE_1	NOCONNECT_26	E16
AM58	SPARE_0	NOCONNECT_27	F14
		NOCONNECT_28	F12
		NOCONNECT_29	H10
T51	NOCONNECT_1	NOCONNECT_30	H14
L14	NOCONNECT_2	NOCONNECT_31	H12
R19	NOCONNECT_3	NOCONNECT_32	A14
E6	NOCONNECT_4	NOCONNECT_33	C14
R17	NOCONNECT_5	NOCONNECT_34	M39
E3	NOCONNECT_6	NOCONNECT_35	P39
D4	NOCONNECT_7	NOCONNECT_36	R39
A60	NOCONNECT_8	NOCONNECT_37	R37
A61	NOCONNECT_9	NOCONNECT_38	C2
BJ2	NOCONNECT_10	NOCONNECT_39	J29
BG1	NOCONNECT_11	NOCONNECT_40	P25
P27	NOCONNECT_12	NOCONNECT_41	R30
A3	NOCONNECT_13	NOCONNECT_42	C63
M10	NOCONNECT_14	NOCONNECT_43	E63
B15	NOCONNECT_15	NOCONNECT_44	D2
		NOCONNECT_45	AP57

Section 7 of 12

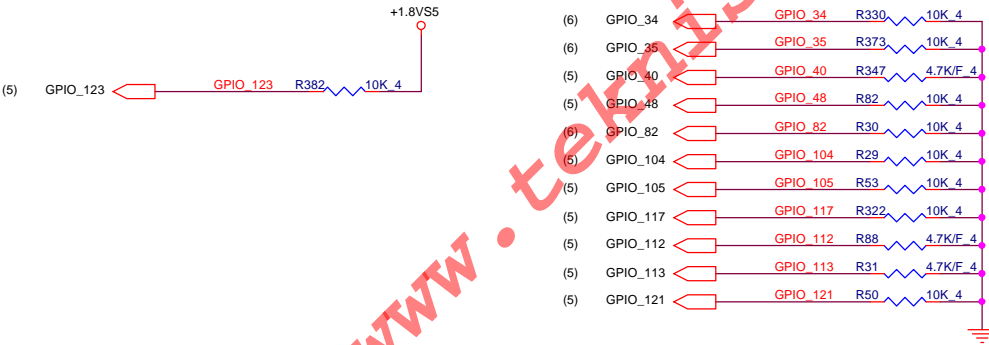


PROJECT : LI8G
Quanta Computer Inc.

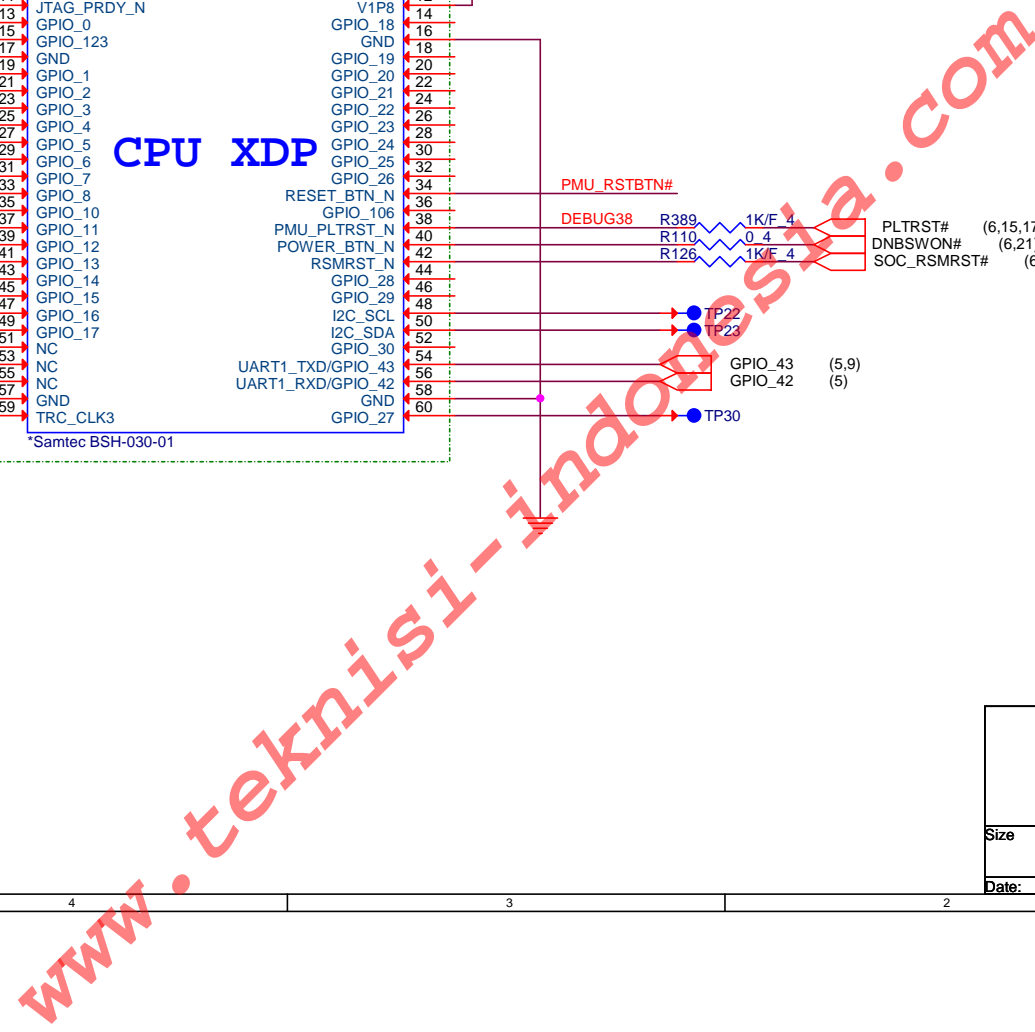


This rail must be 1.24V for A0 step.
Starting B-step, this rail can be 1.24V or 1.35V

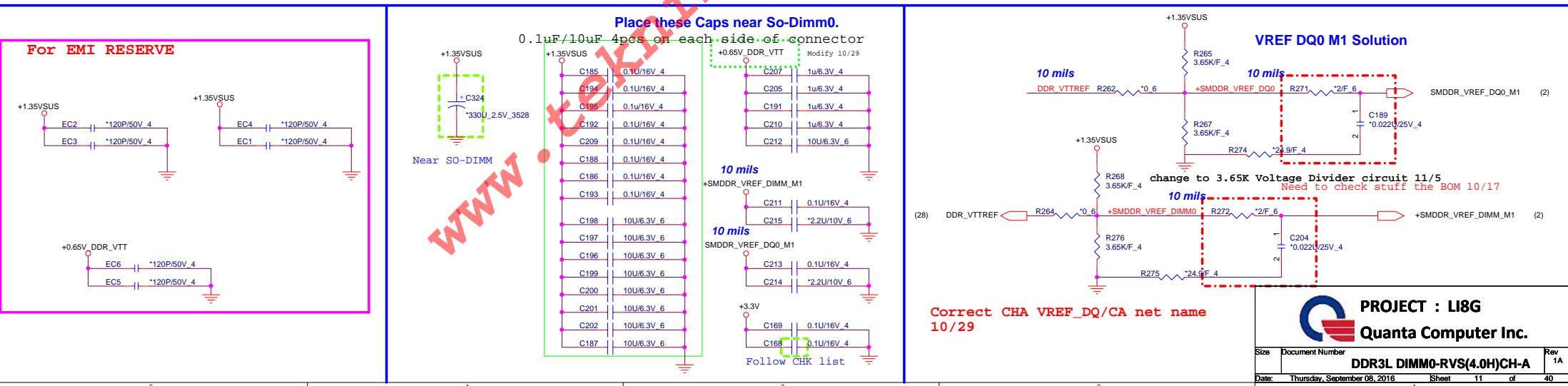
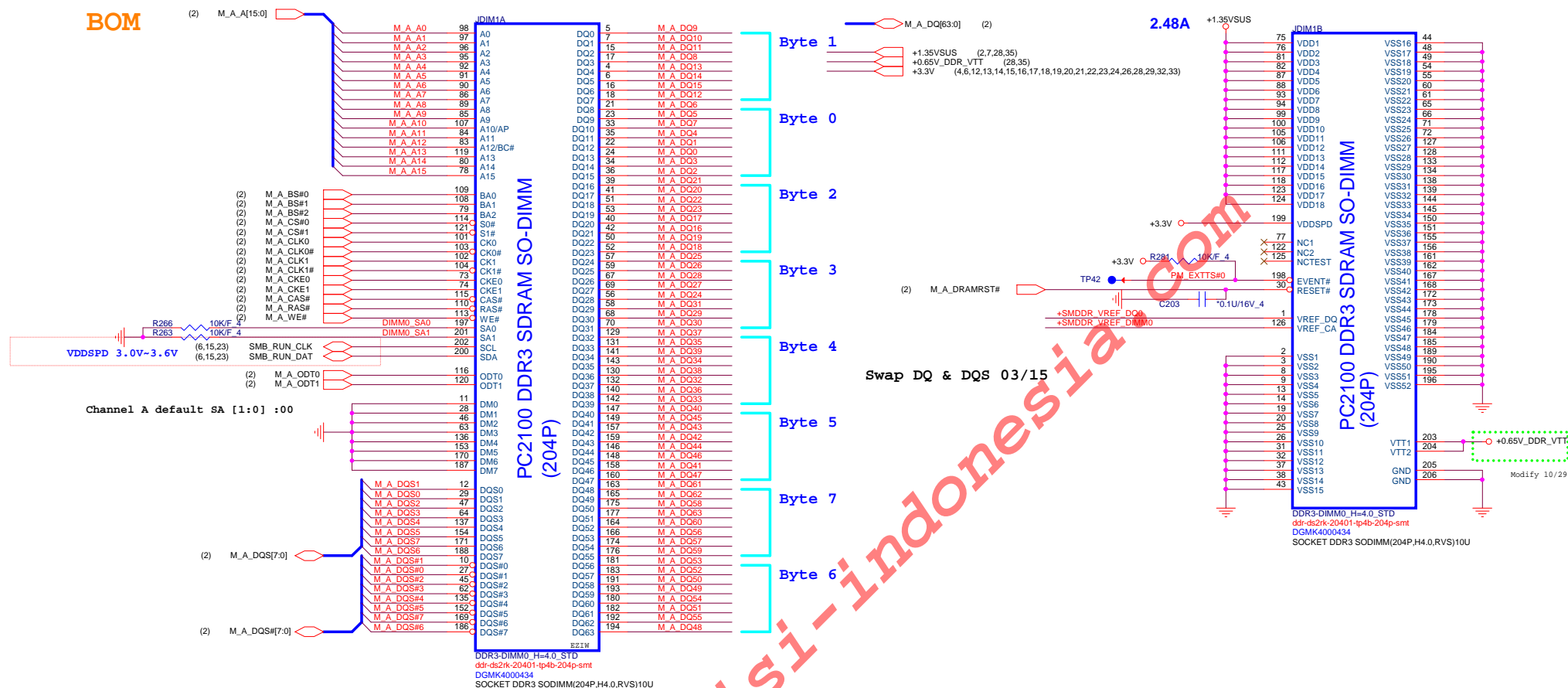
Hardware Strap	Strap Description	Value
GPIO_36	VCC_1P24V_1P35V_A voltage select 0 = 1.24V 1 = 1.35V	0
GPIO_39	Enable CSE(TXE3.0) ROM Bypass 0 = Disable bypass 1 = Enable Bypass	0
GPIO_43	Allow eMMC as a boot source 0 = Disable 1 = Enable	0
GPIO_44	Allow SPI as a boot source 0 = Disable 1 = Enable	1
GPIO_47	Force DNX FW Load 0 = Do not force 1 = Force	0
GPIO_78	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V	0
GPIO_88	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
GPIO_92	SMBus No Re-Boot 0 = Disable (default) 1 = Enable	0
GPIO_110	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
GPIO_111	Boot BIOS Strap 0 = Boot from SPI 1 = Do not boot from SPI	0
GPIO_120	Top swap override 0 = Disable 1 = Enable	0



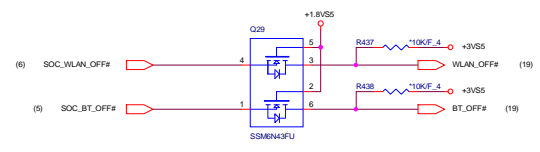
Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_40/GPIO_48/GPIO_104/GPIO_105/GPIO_112/GPIO_113/GPIO_117/GPIO_121 PD
GPIO_106/GPIO_123 PU



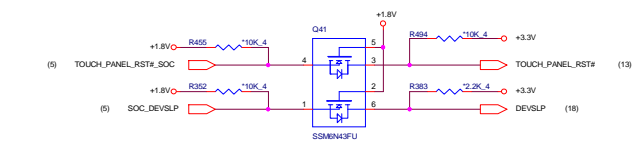
BOM



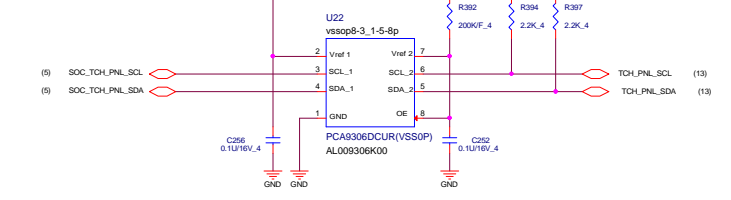
RF OFF#



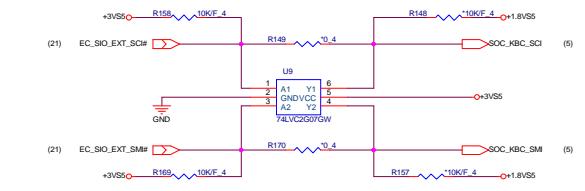
TCH_RST#/DEVSLP



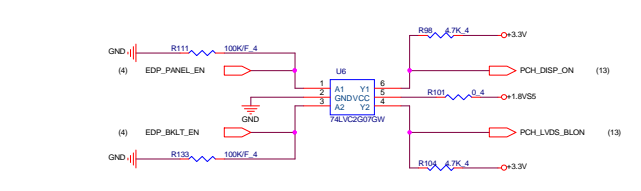
Touch Panel I2C(OK)



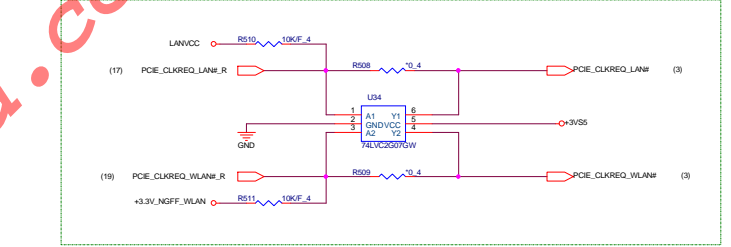
SCI#/SMI#(OK)



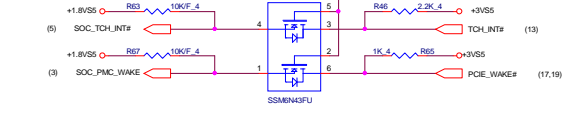
Disp ON/BL ON(OK)



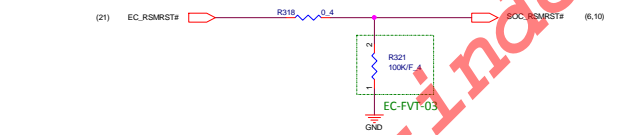
CLKREQ#

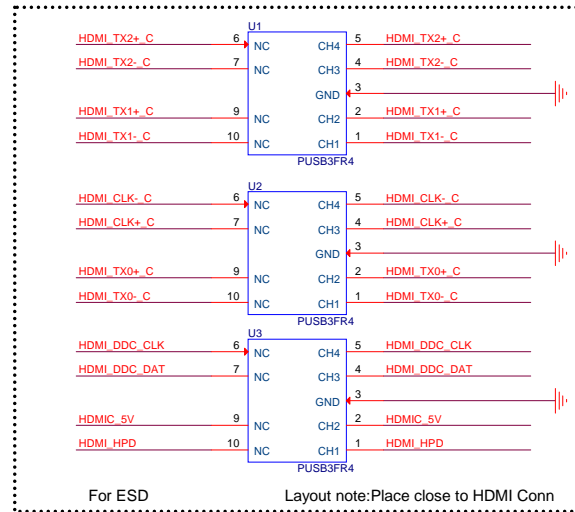
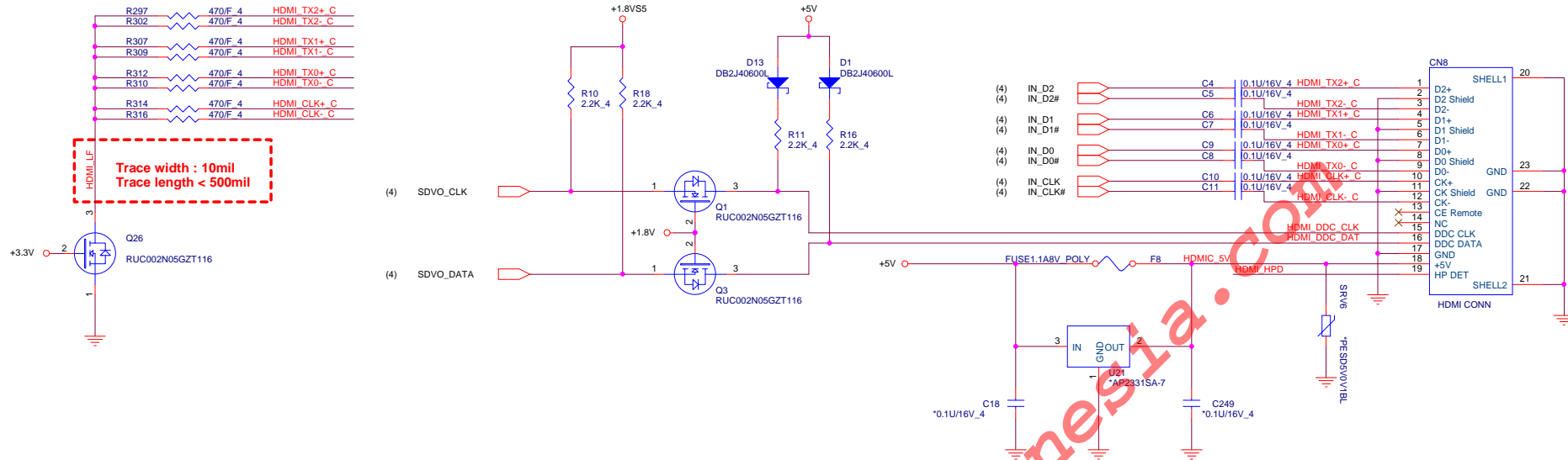


INT

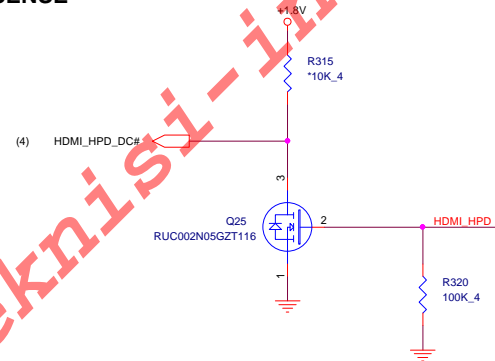


RSMRST#(OK)



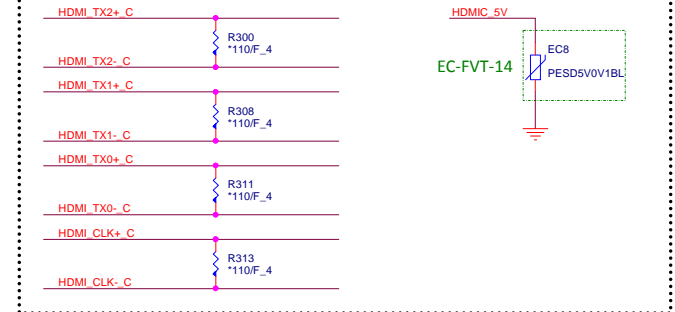


HDMI HPD SENSE



Note: It is highly recommended a passgate N-MOSFET device is selected that has Gate Threshold Voltage $\leq 1.5V$.
Note: It's required to enable internal 20K PU resistor on these HV_DDIx_HPDC signals by BIOS

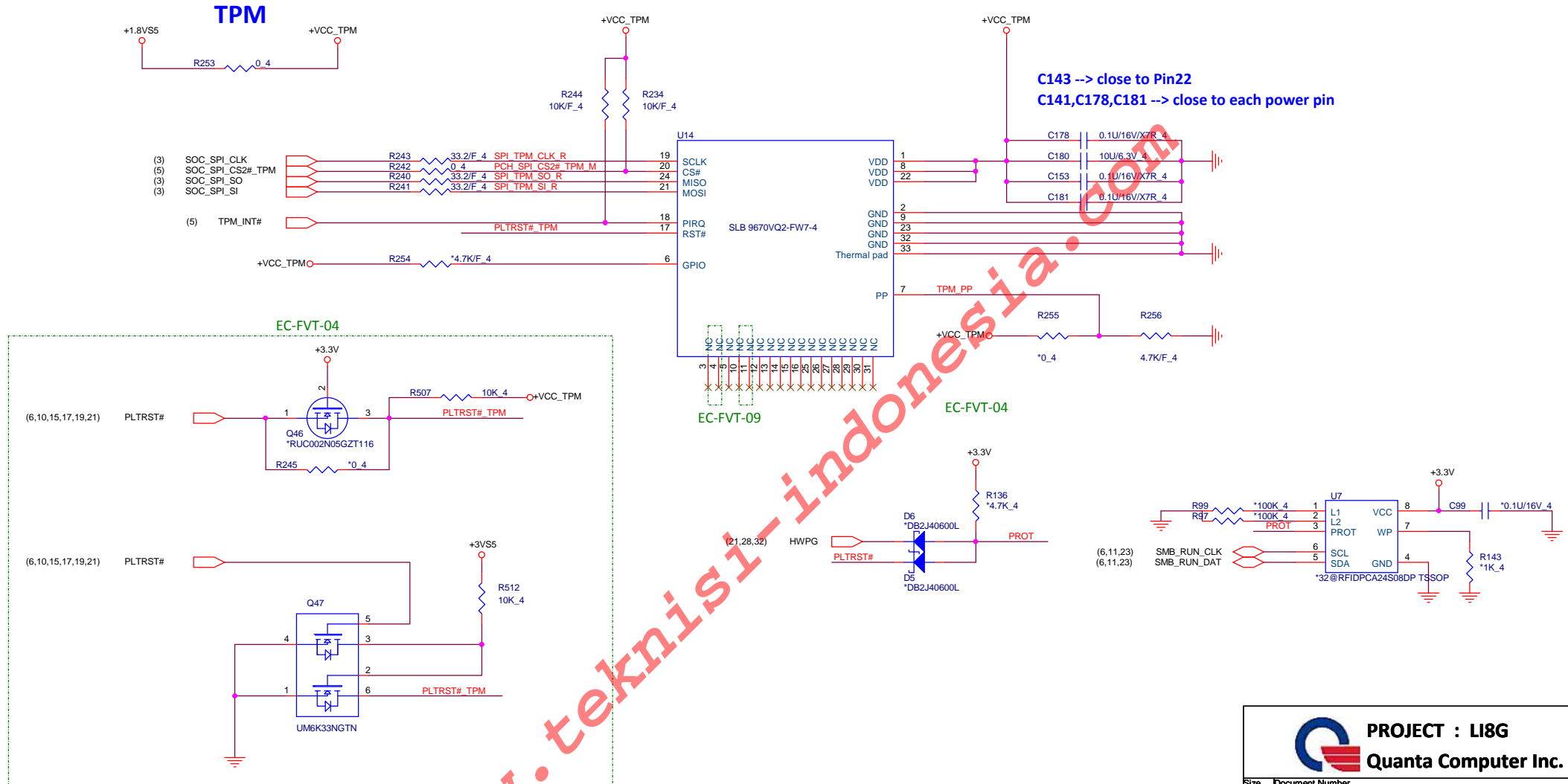
EMI reserve for HDMI



PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI CONN	1A
Date:	Thursday, September 08, 2016	Sheet 14 of 40

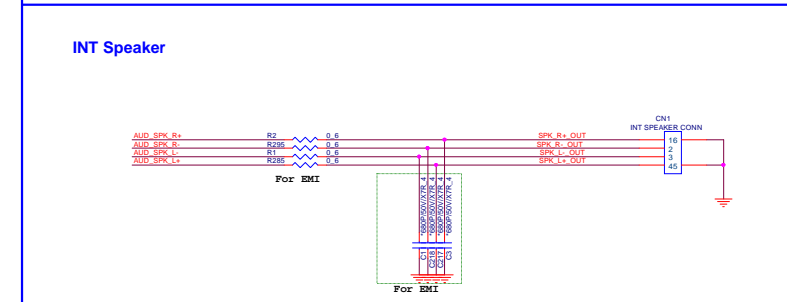
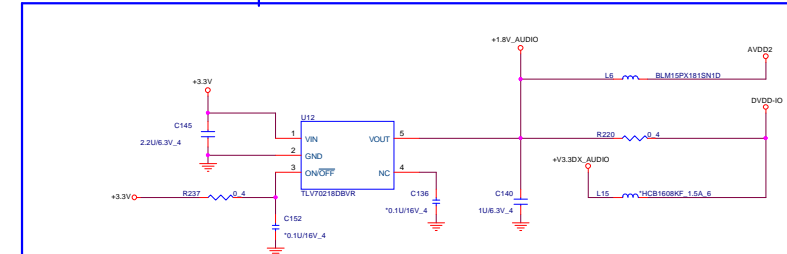
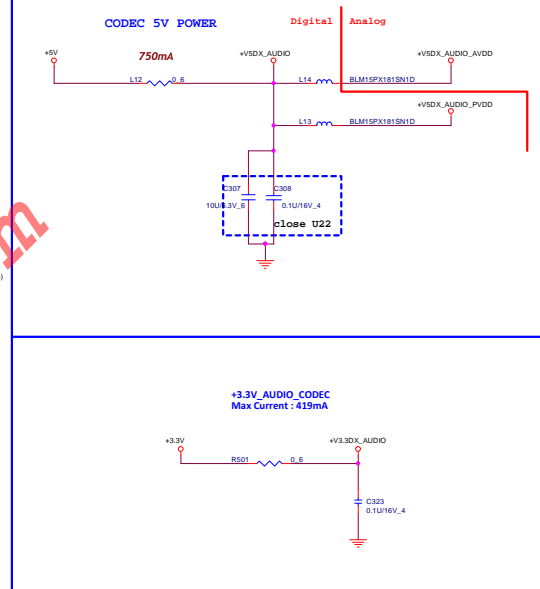
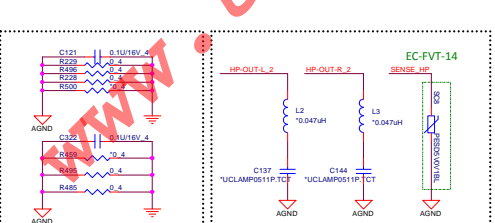
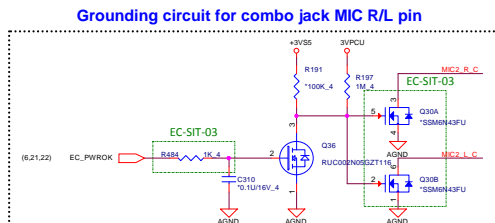
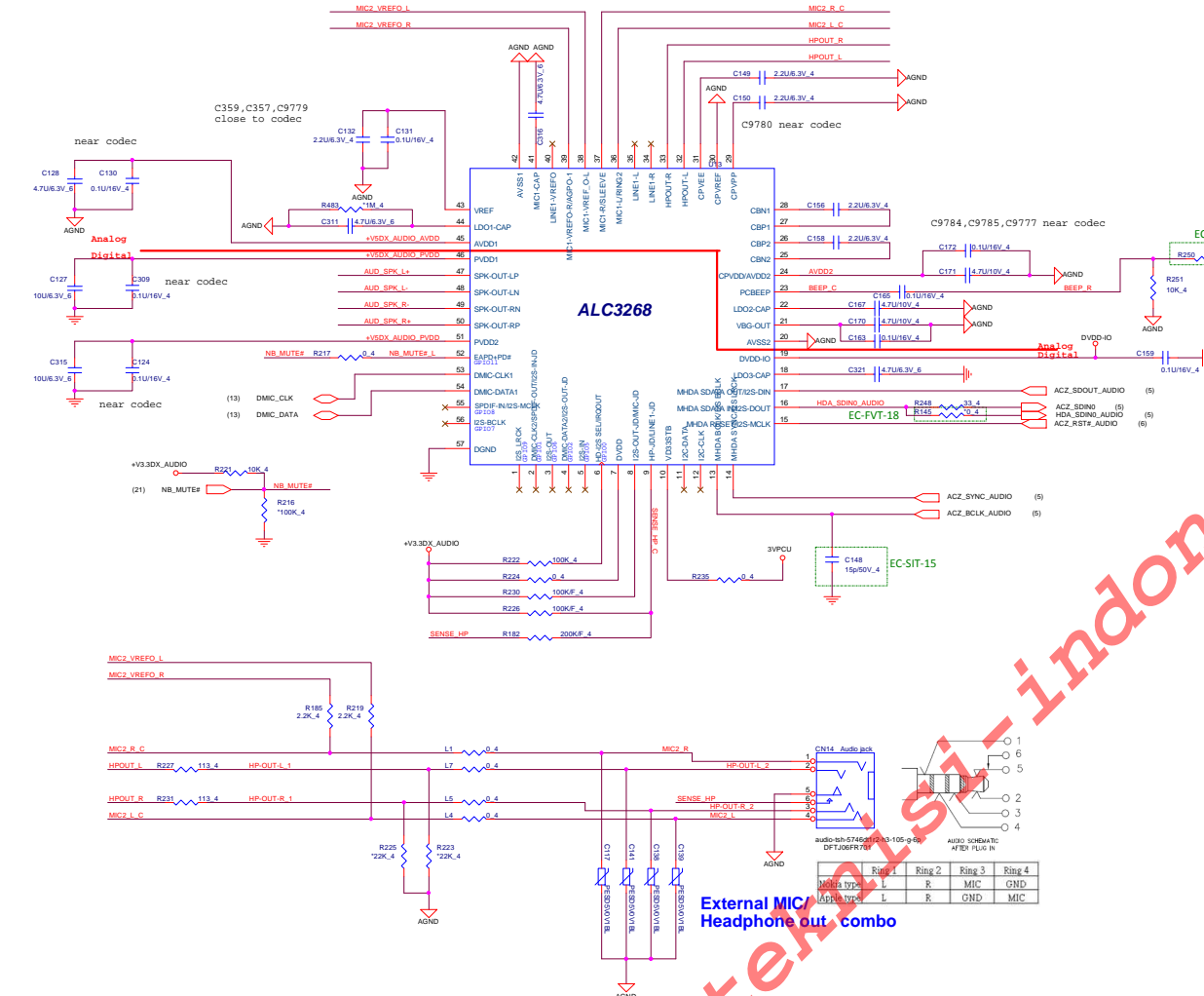
HDMI CONN

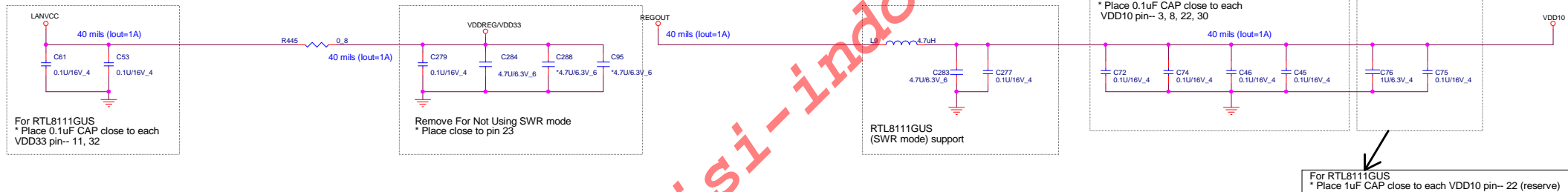
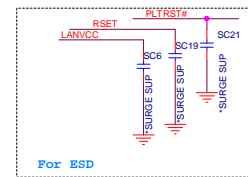
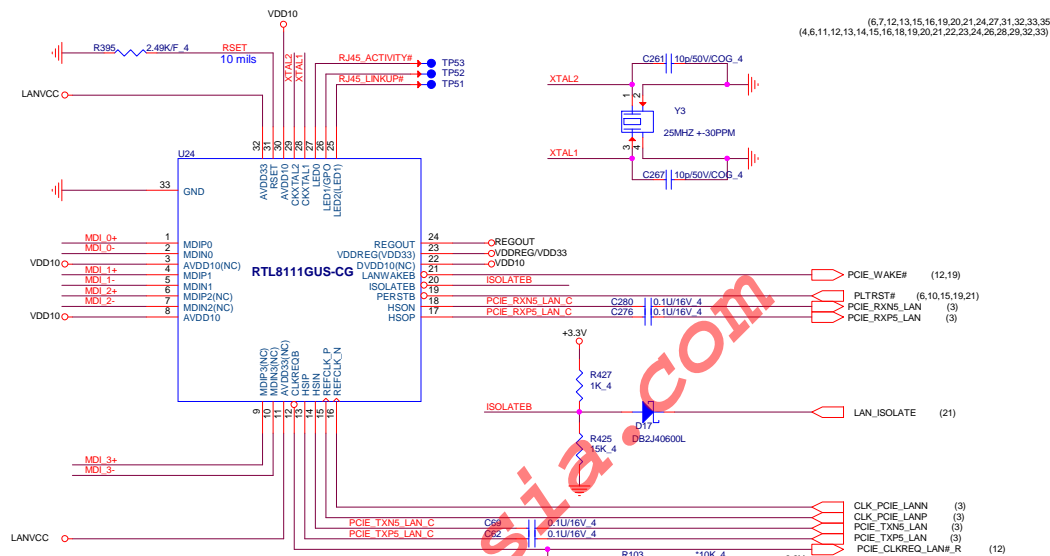
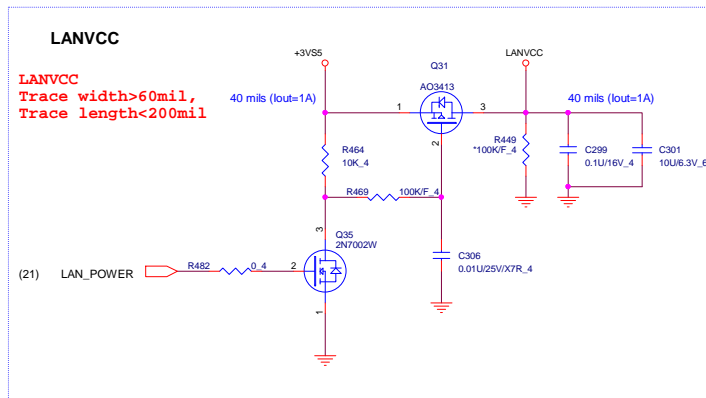


PROJECT : LI8G
Quanta Computer Inc.

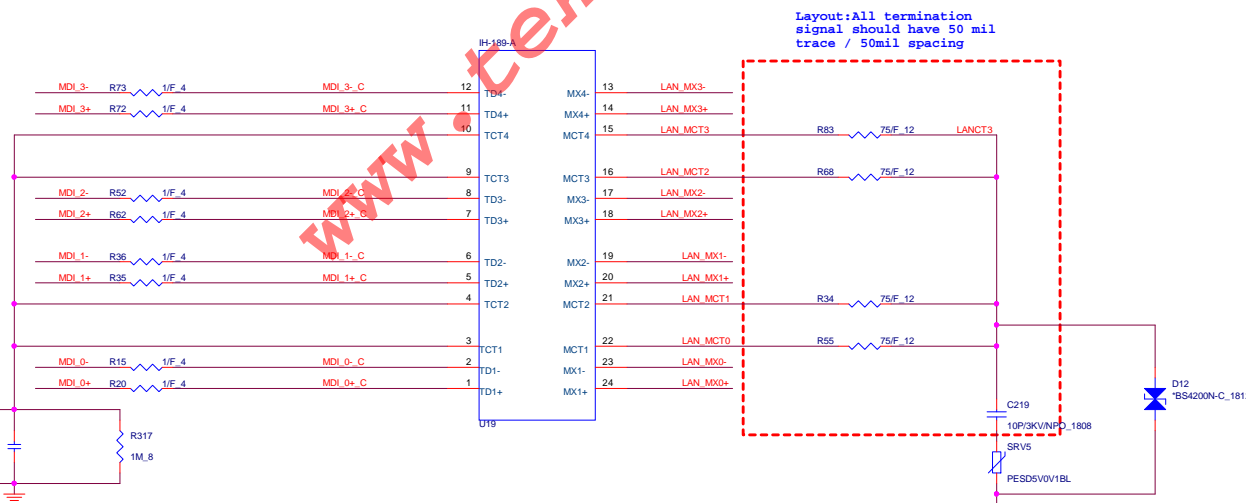
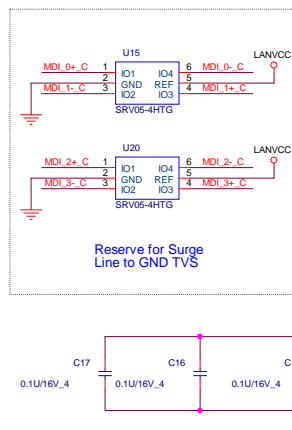
Size	Document Number	Rev
	TPM/RFID	1A
Date:	Thursday, September 08, 2016	Sheet 15 of 40

ALC3268

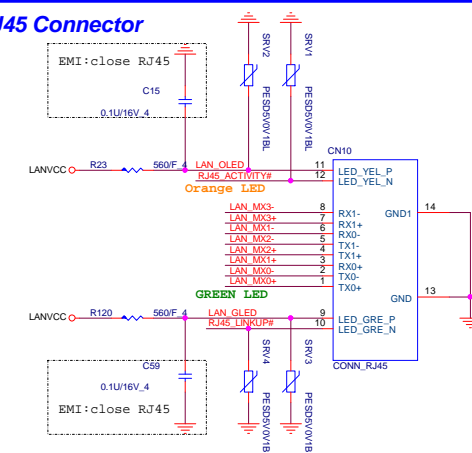


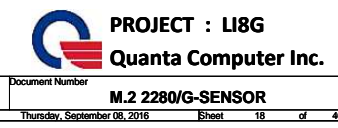
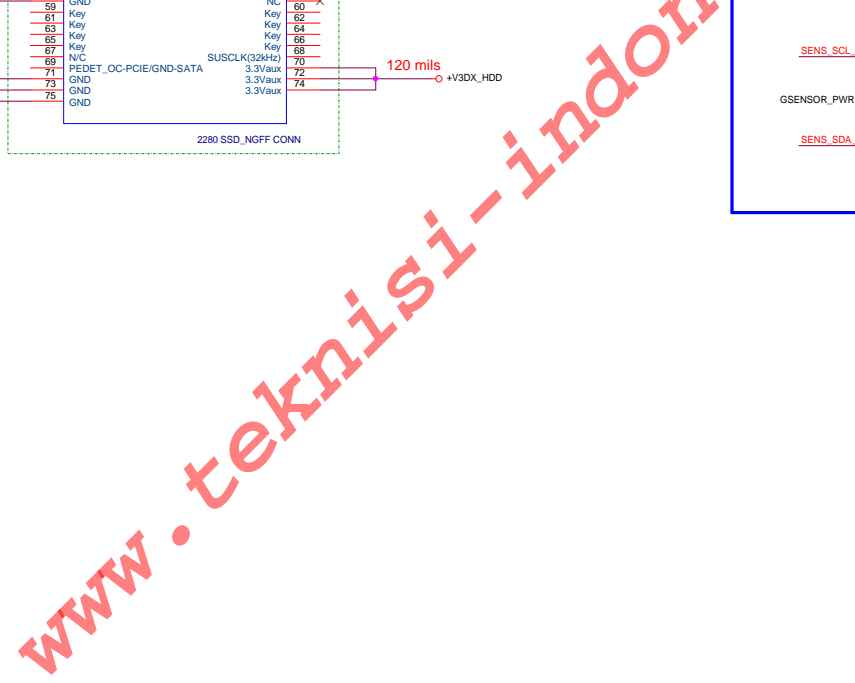


Transformer

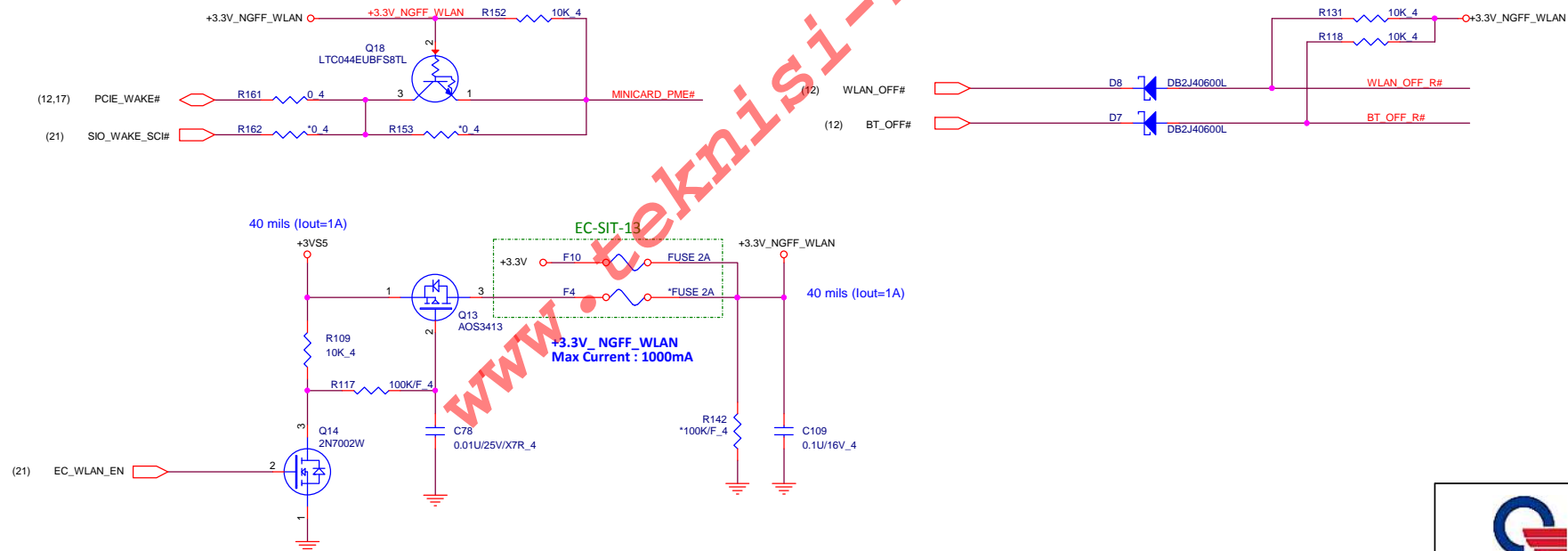
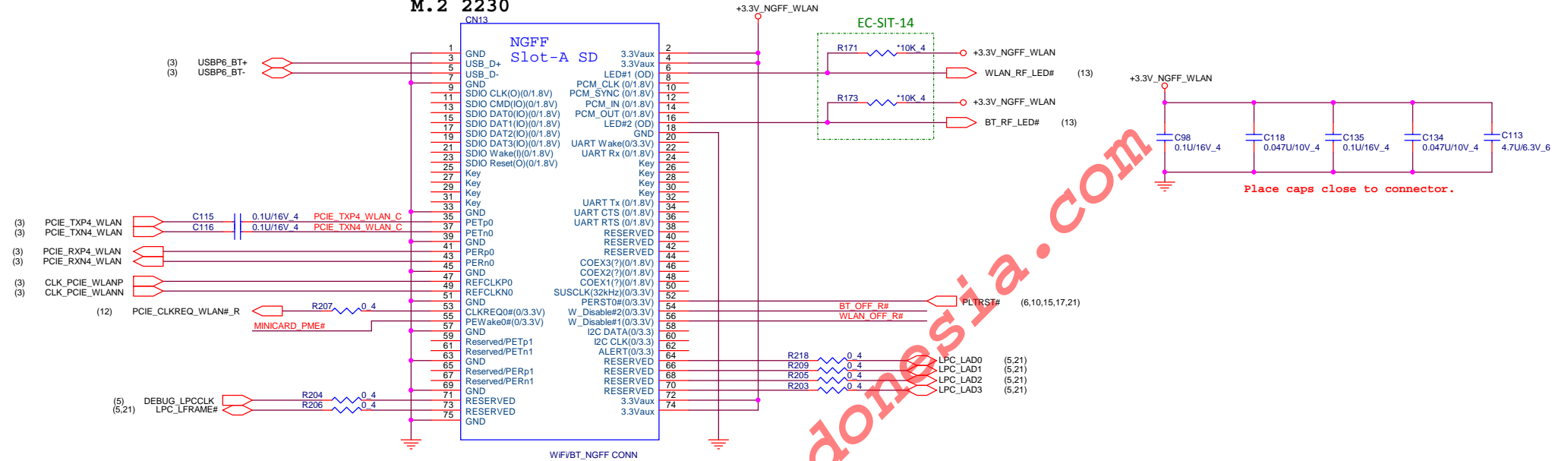


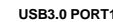
RJ45 Connector





NGFF WiFi/BT connector M.2 2230

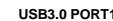
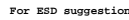


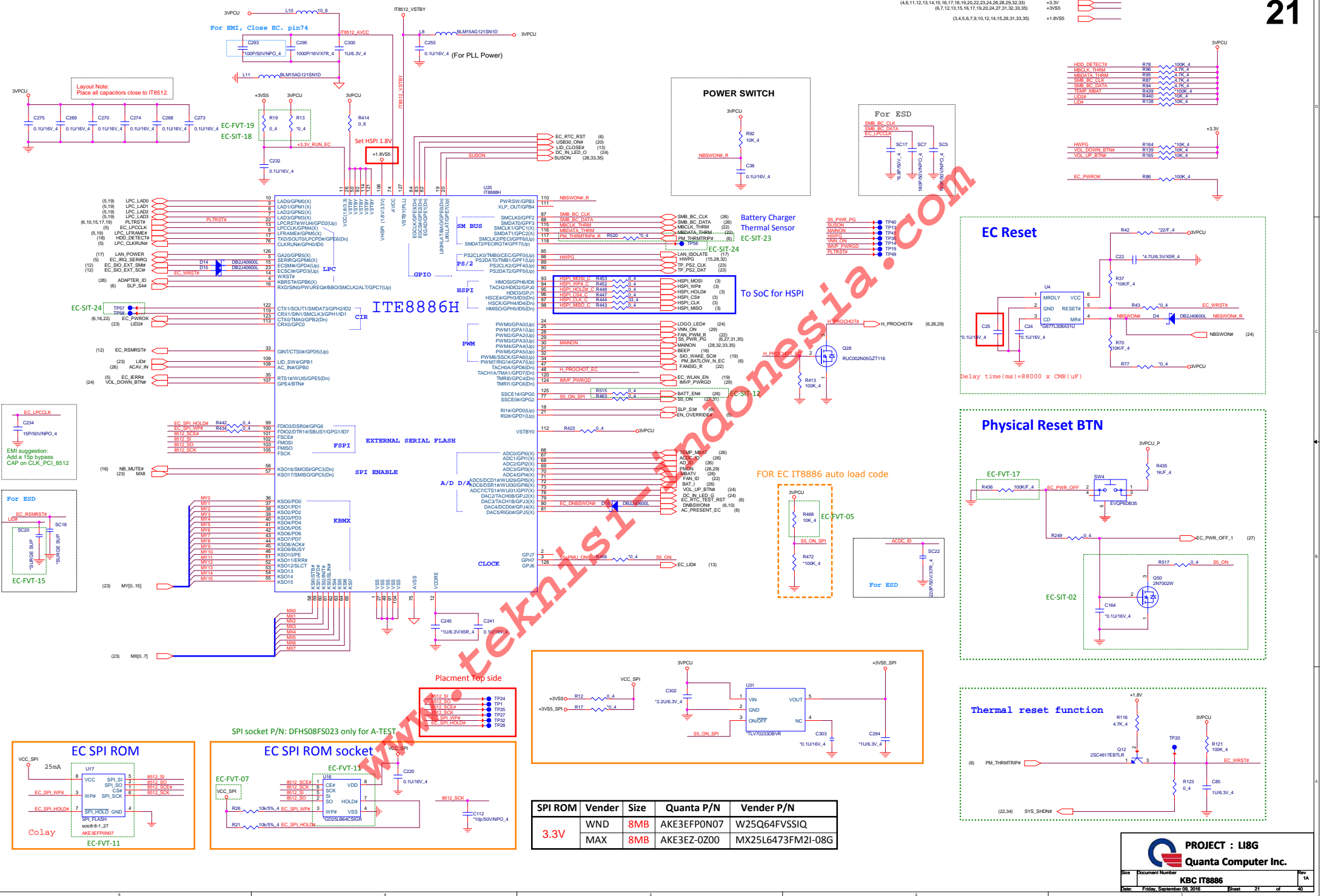


60 mils (Iout=1.5A)

C286

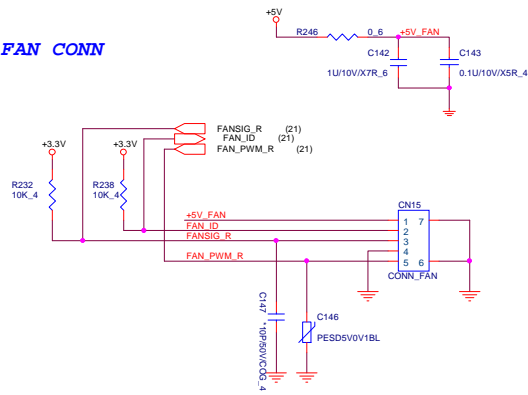
C287



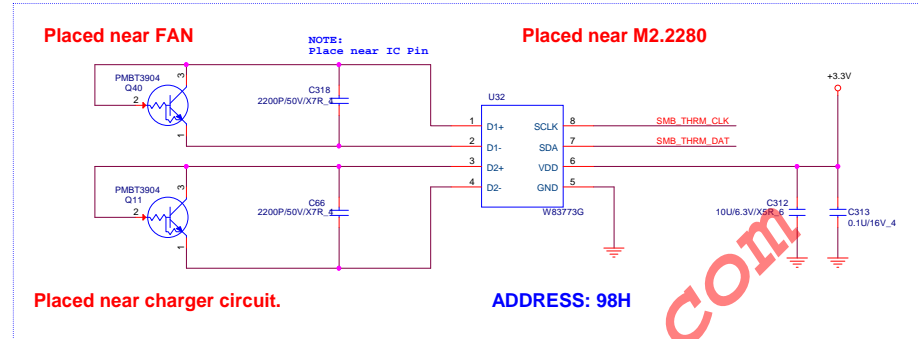


SPI ROM	Vender	Size	Quanta P/N	Vender P/N
3.3V	WND	8MB	AKE3EFP0N07	W25Q64FVSSIQ
	MAX	8MB	AKE3EZ-0Z00	MX25L6473FM2I-08G

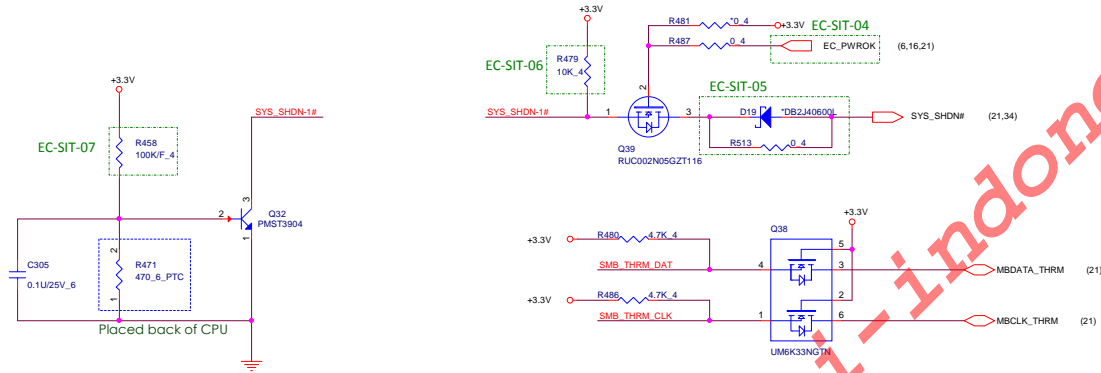
FAN CONN



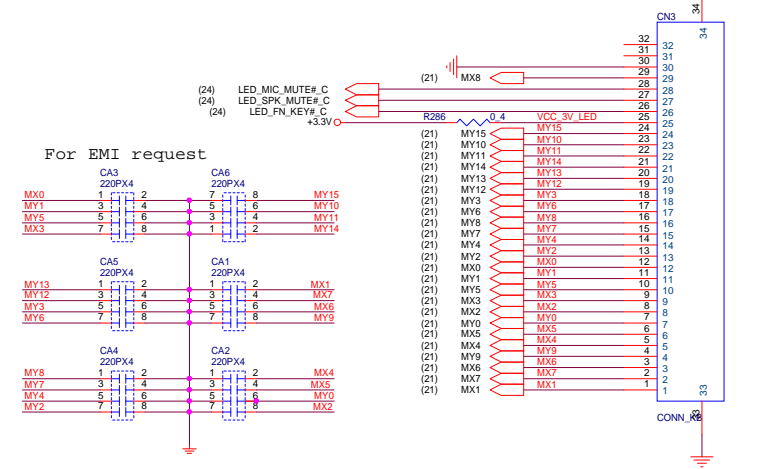
Thermal Sensor



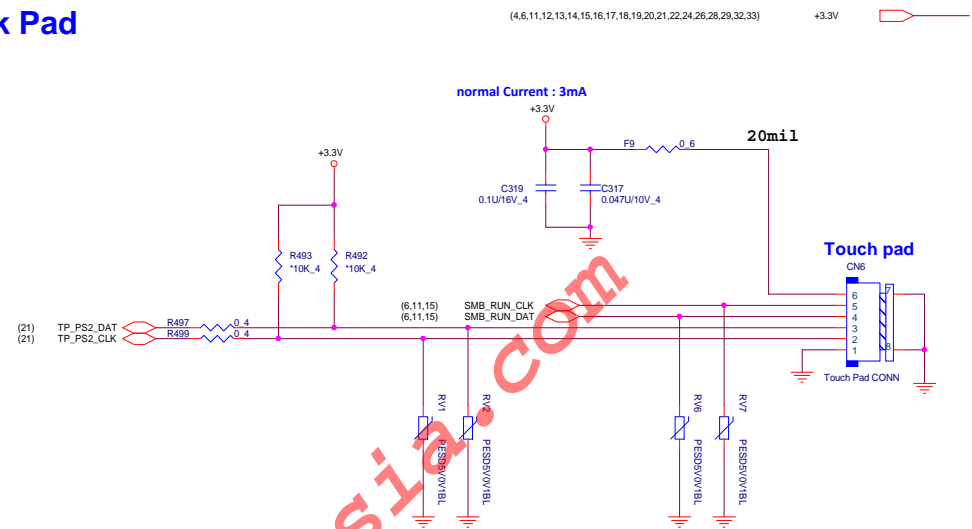
CPU PTC circuit



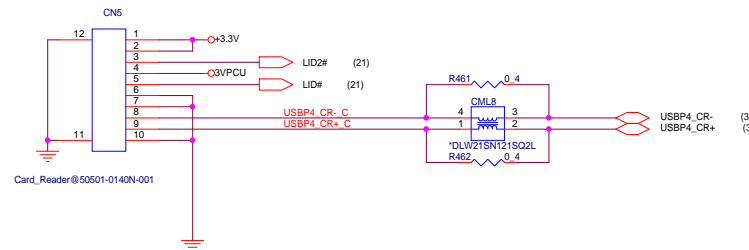
KEYBOARD



Click Pad



To Card Reader Board



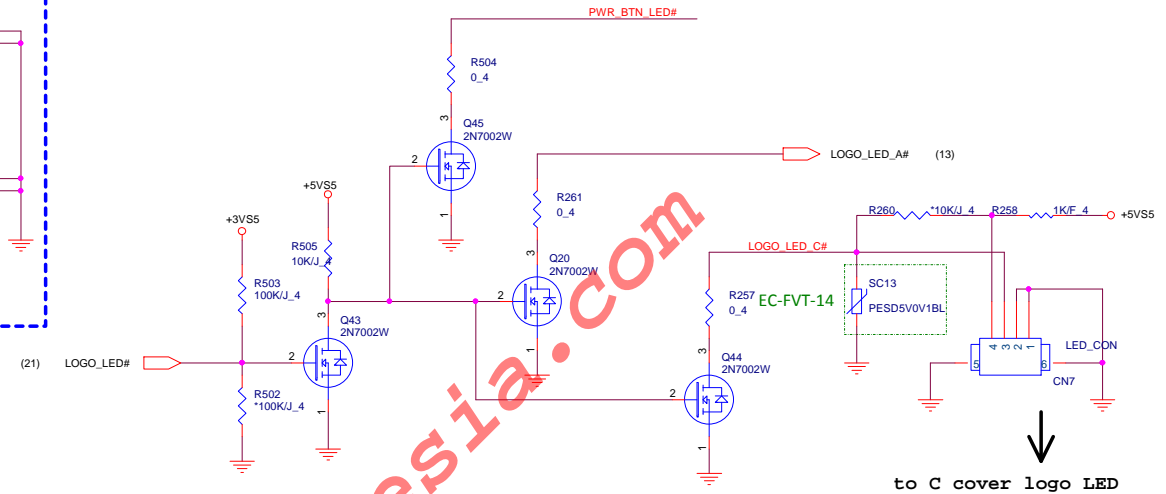
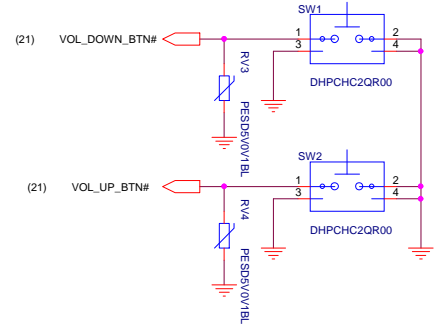
www.teknisi-indonesia.com



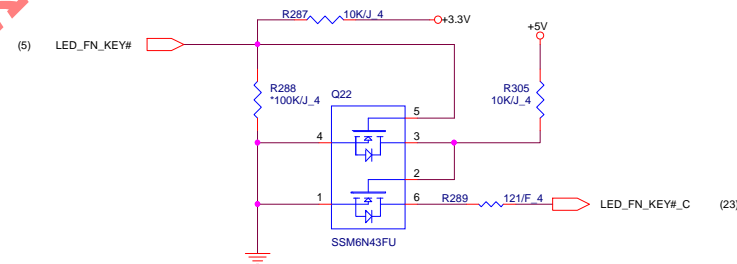
PROJECT : LI8G
Quanta Computer Inc.

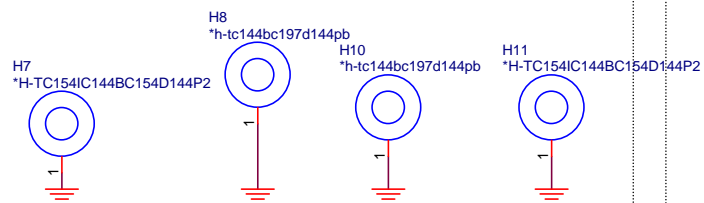
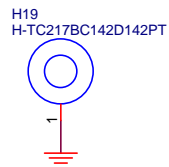
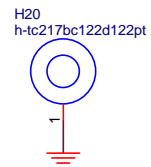
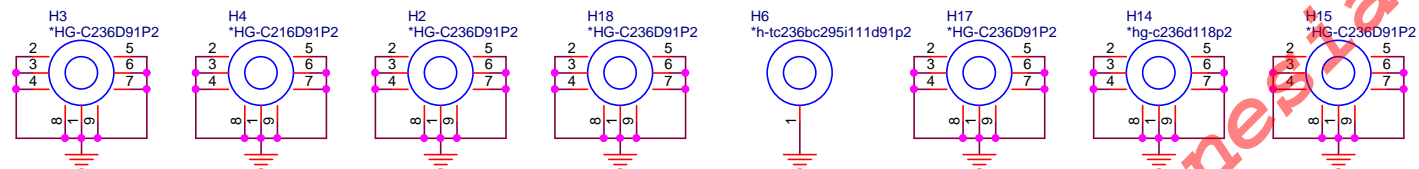
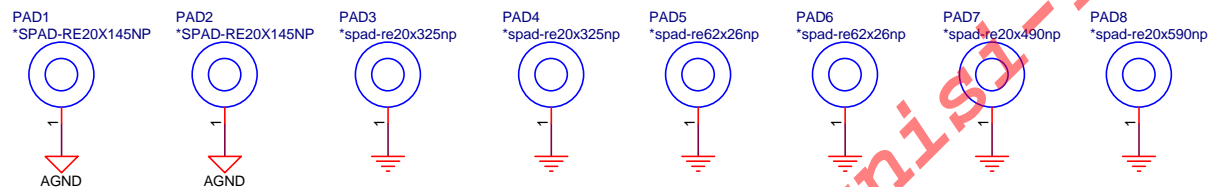
Size	Document Number	Rev
	KB/TP/DB	1A
Date: Thursday, September 08, 2016	Sheet 23 of 40	

Volume up/down Switch

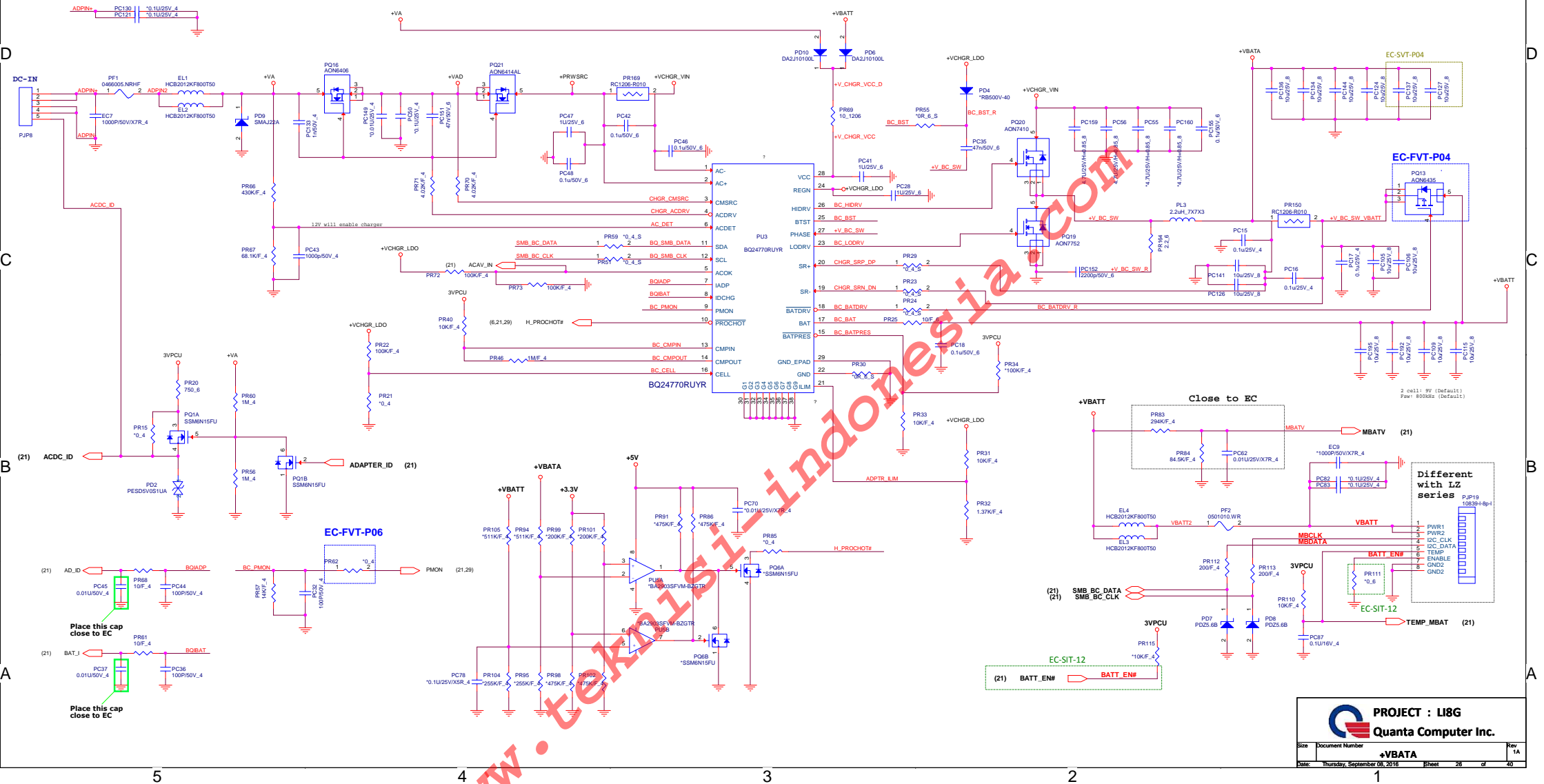
[illegible]

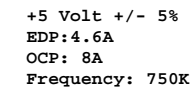
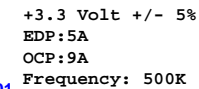
Fn key LED

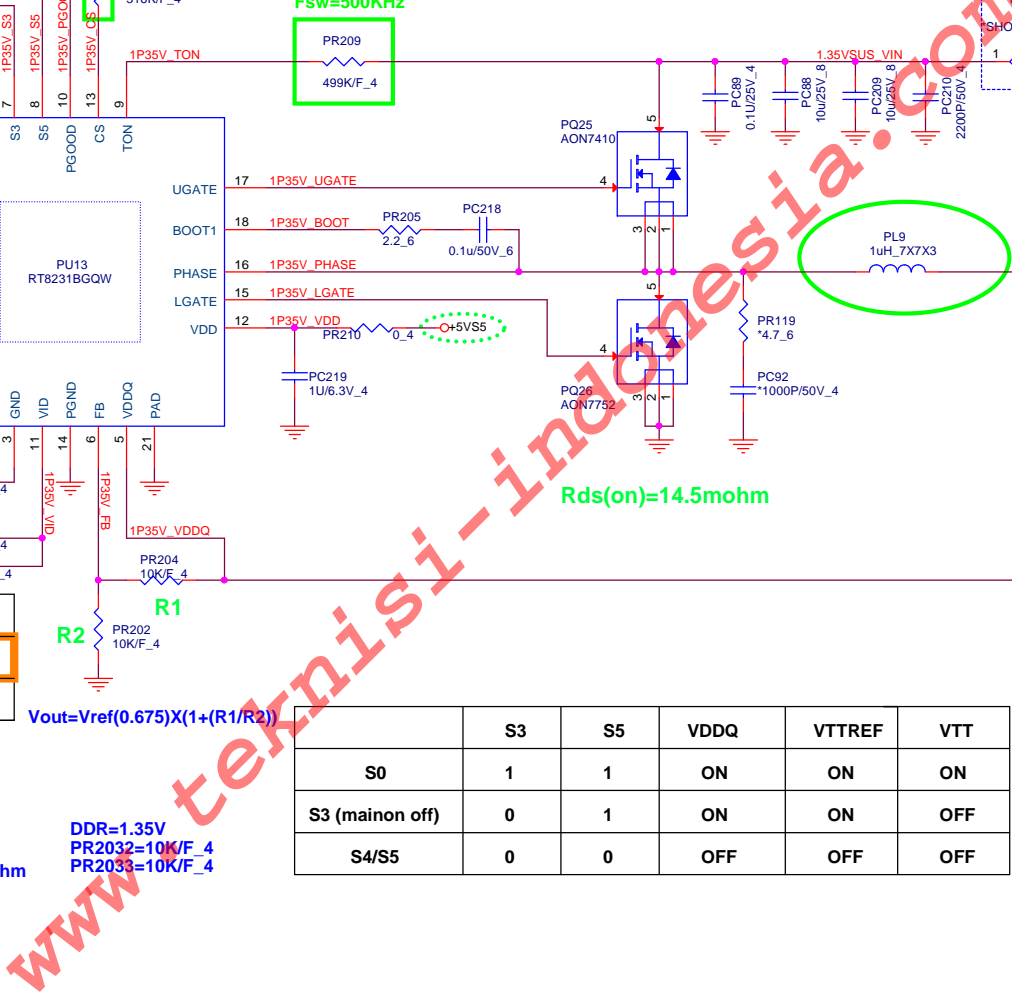


Hole For CPU bracket**NGFF WLAN****NGFF M.2 2280****Boundary Hole****PAD****Non-PTH Hole**

PROJECT : LI8G
Quanta Computer Inc.

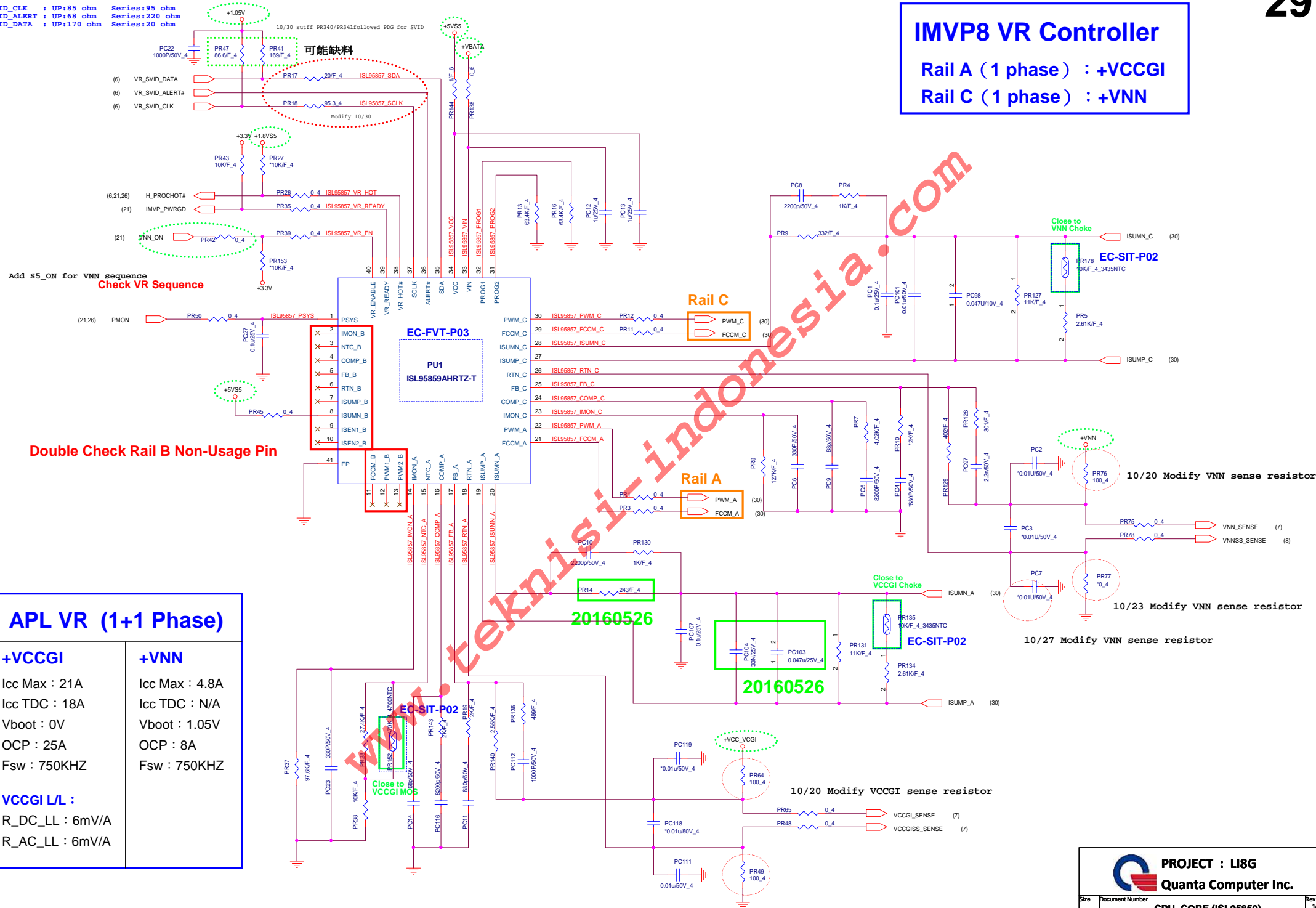






Change pull up to +1.05V_S5

```
SVID_CLK      : UP:85 ohm      Series:95 ohm
SVID_ALERT    : UP:68 ohm      Series:220 ohm
SVID_DATA     : UP:170 ohm     Series:20 ohm
```



APL VR (1+1 Phase)

+VCCGI

Icc Max : 21A
Icc TDC : 18A
Vboot : 0V
OCP : 25A
Fsw : 750KHZ

+VNN

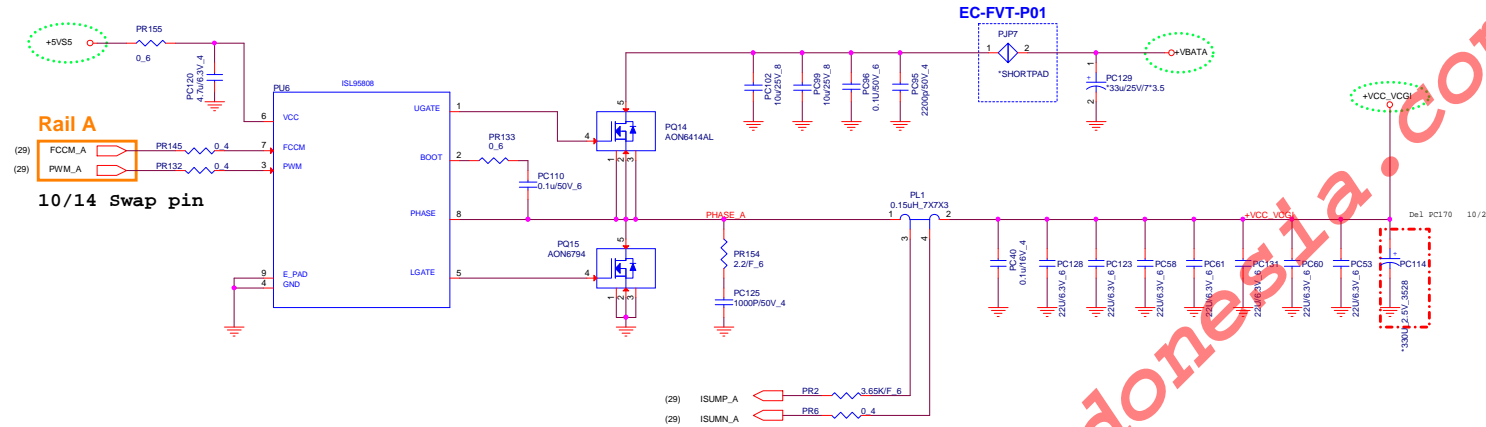
Icc Max : 4.8A
Icc TDC : N/A
Vboot : 1.05V
OCP : 8A
Fsw : 750KHZ

VCCGI L/L :

R_DC_LL : 6mV/A
R_AC_LL : 6mV/A

(13,26,27,28,29,34,35) +VBATA
 (7,29) +VCC_VCGI
 (7,29) +VNN
 (13,20,24,27,28,29,33,35) +5VS5

VCCGI



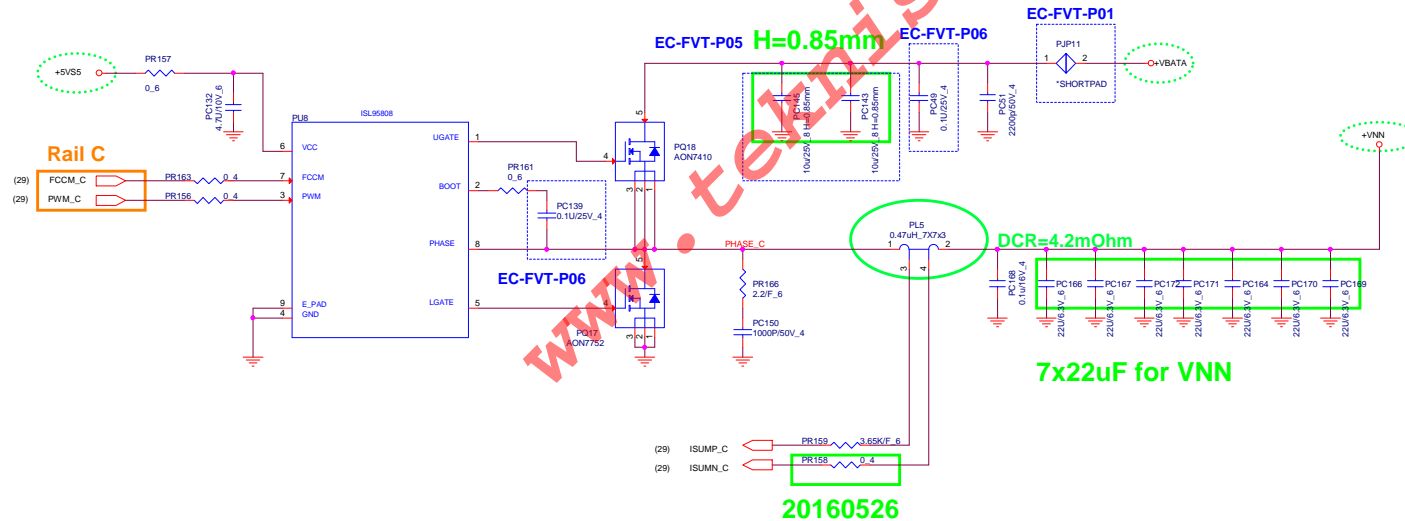
+VCCGI

Icc Max : 21A
 Icc TDC : 18A
 Vboot : 0V
 OCP : 25A
 Fsw : 750KHZ

VCCGI L/L :

R_DC_LL : 6mV/A
 R_AC_LL : 6mV/A

VNN



+VNN

Icc Max : 4.8A
 Icc TDC : N/A
 Vboot : 1.05V
 OCP : 8A
 Fsw : 750KHZ



PROJECT : LI8G
Quanta Computer Inc.

Size Document Number
 Date: Friday, September 09, 2016 Sheet 30 of 40

+VCCGI / +VNN

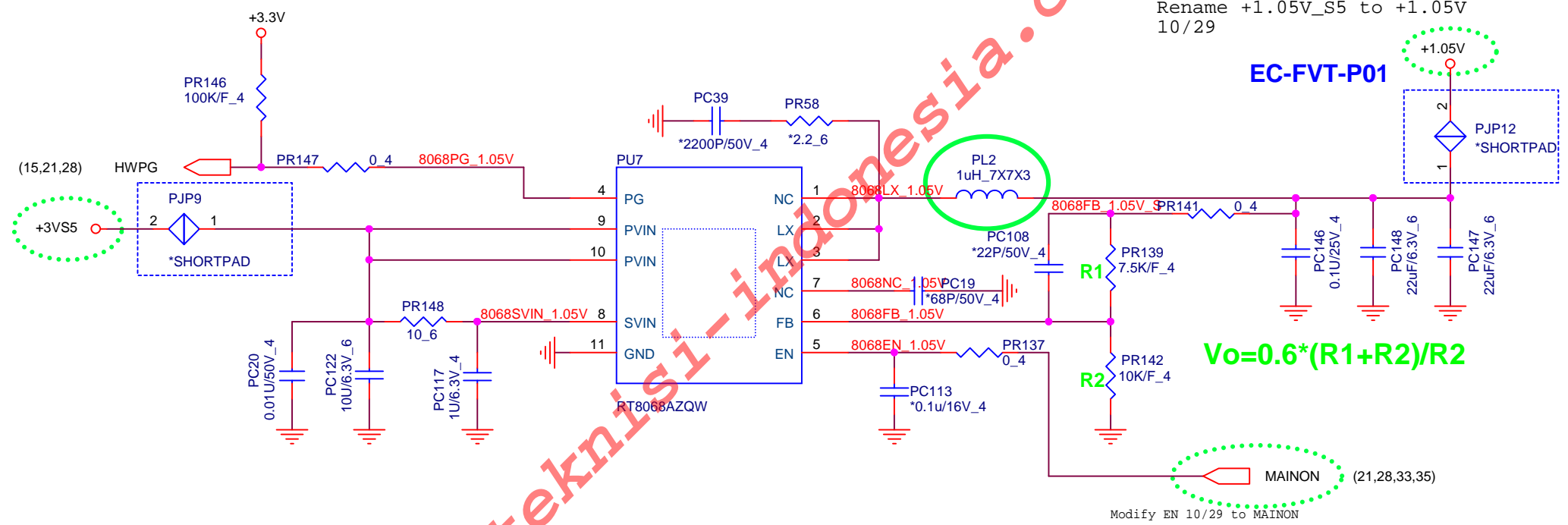
Rev
 1A


+1.05V_S5
1.05Volt +/- 5%
TDC : 2.025A
PEAK : 2.7A
Width : 100mil

Rename +1.05V_S5 to +1.05V
10/29

EC-FVT-P01

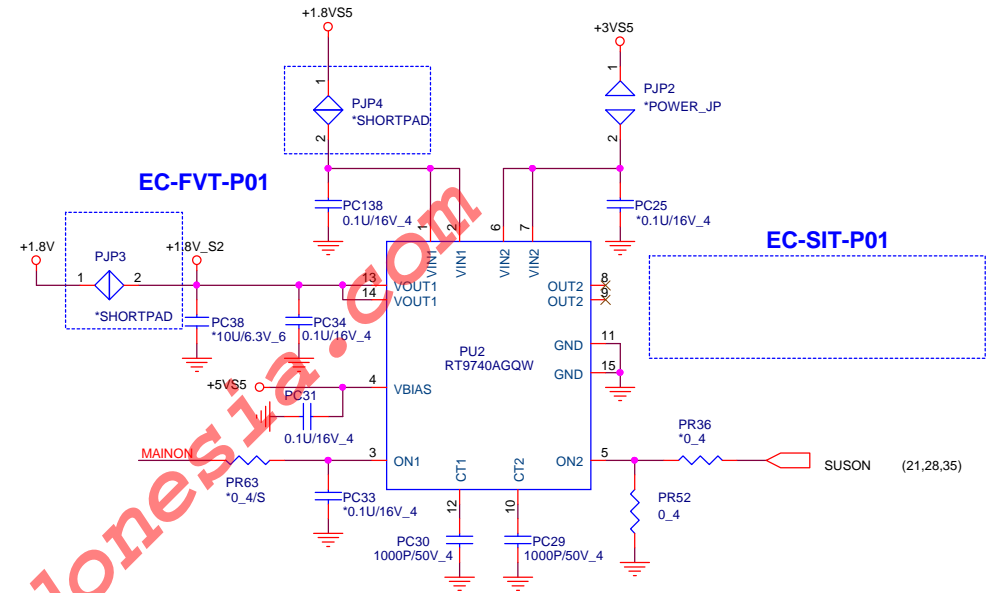
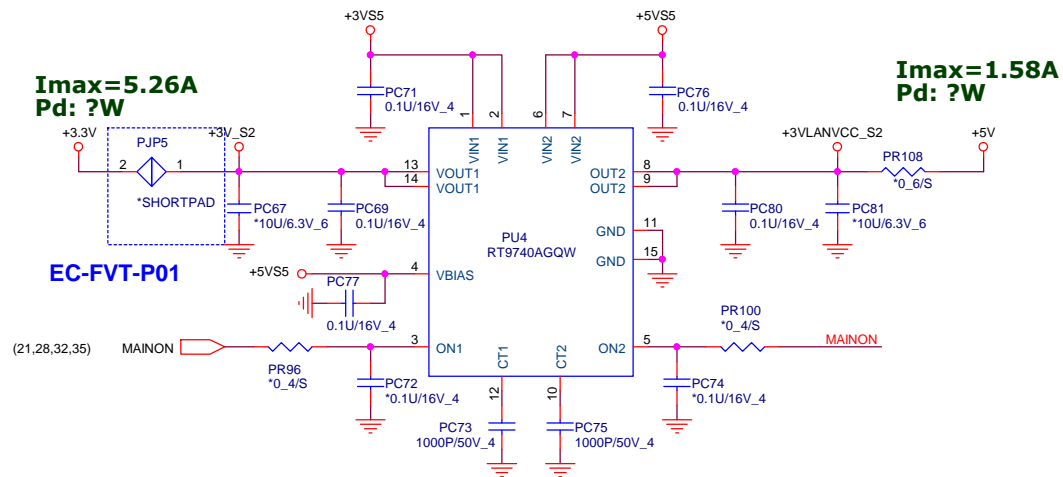
$$Vo=0.6*(R1+R2)/R2$$





PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	+1.05V (RT8068AZQW)	1A
Date:	Thursday, September 08, 2016	Sheet 32 of 40

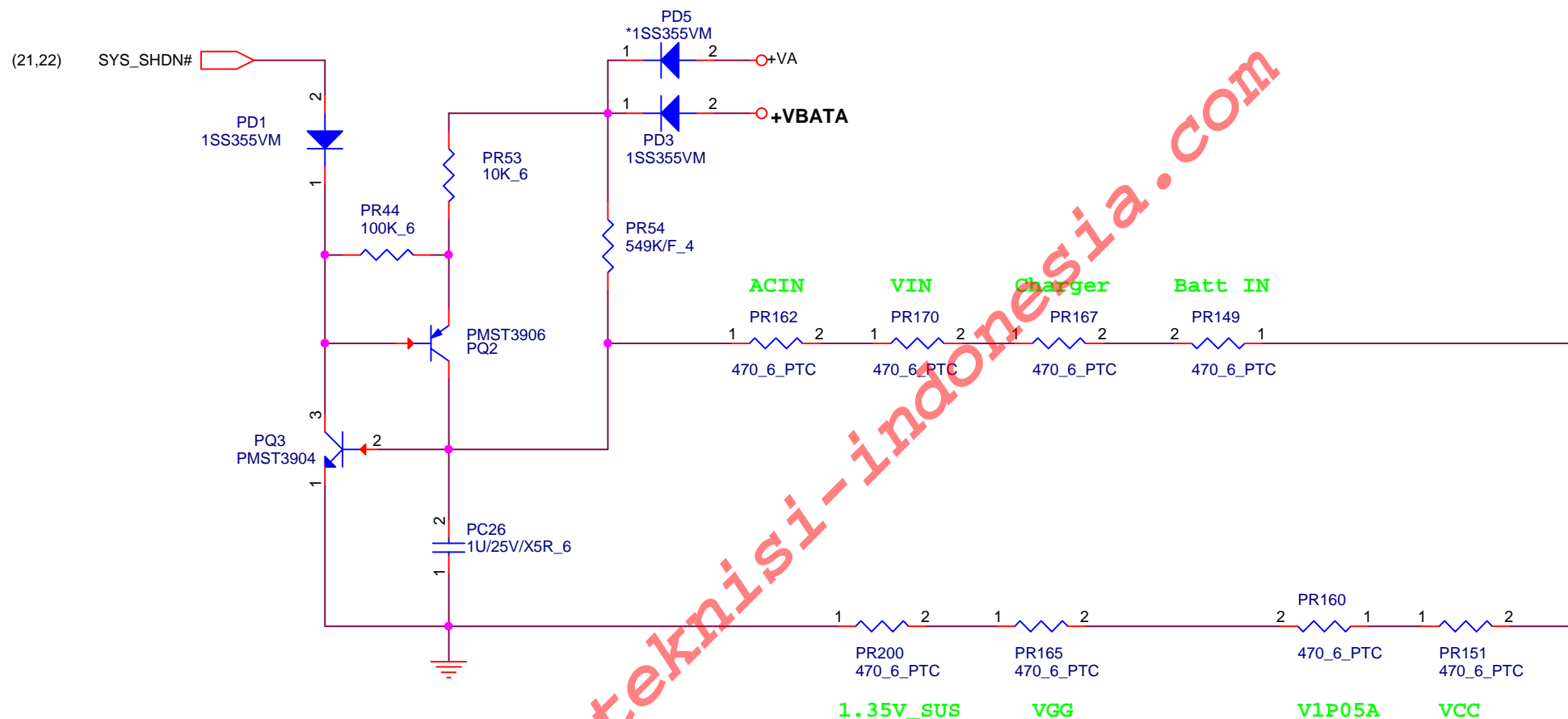


www.teknisi-indonesia.com



PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	Load SW	1A
Date:	Thursday, September 08, 2016	Sheet 33 of 40



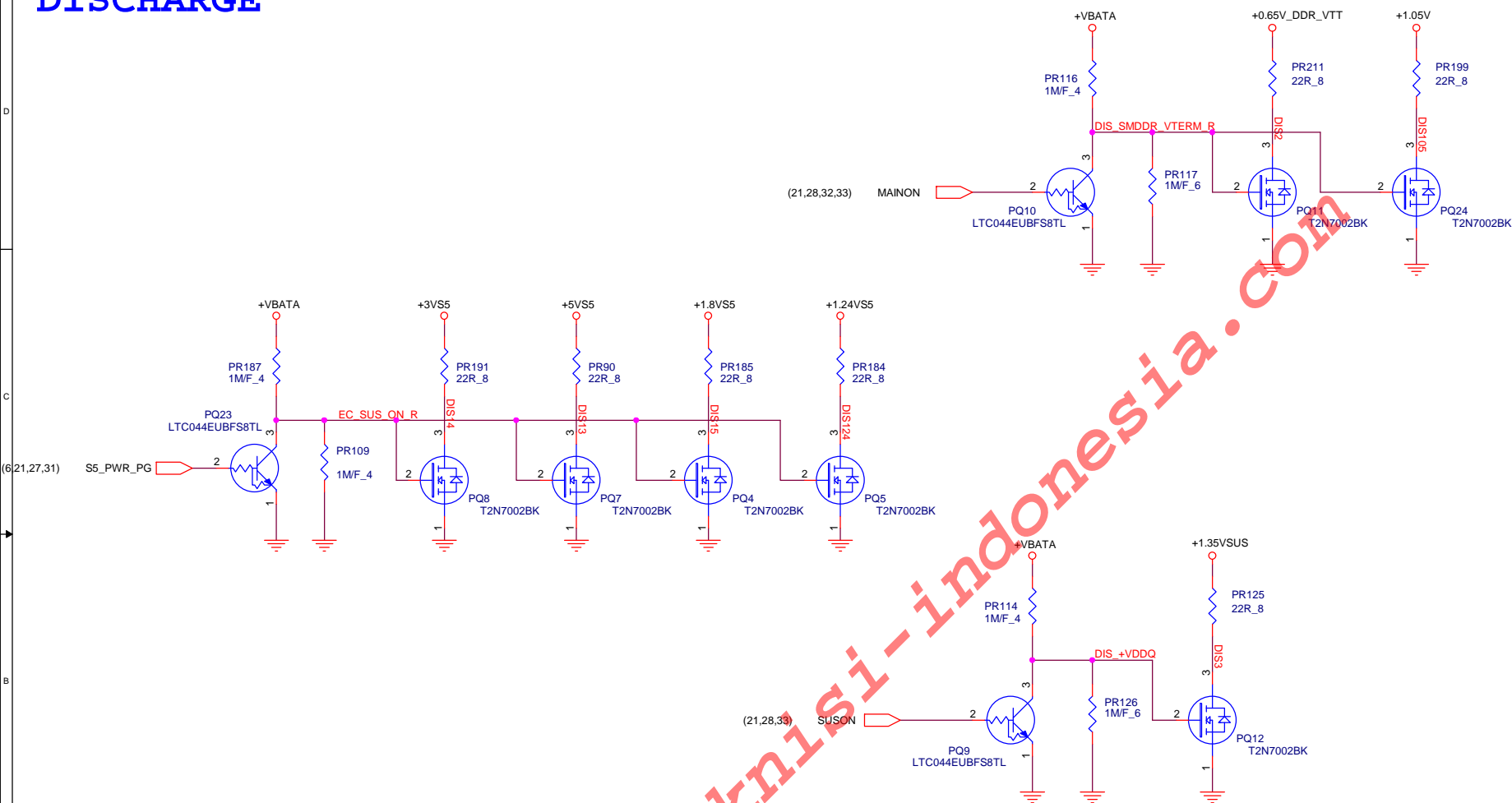
www.teknisi-indonesia.com



PROJECT : LI8G

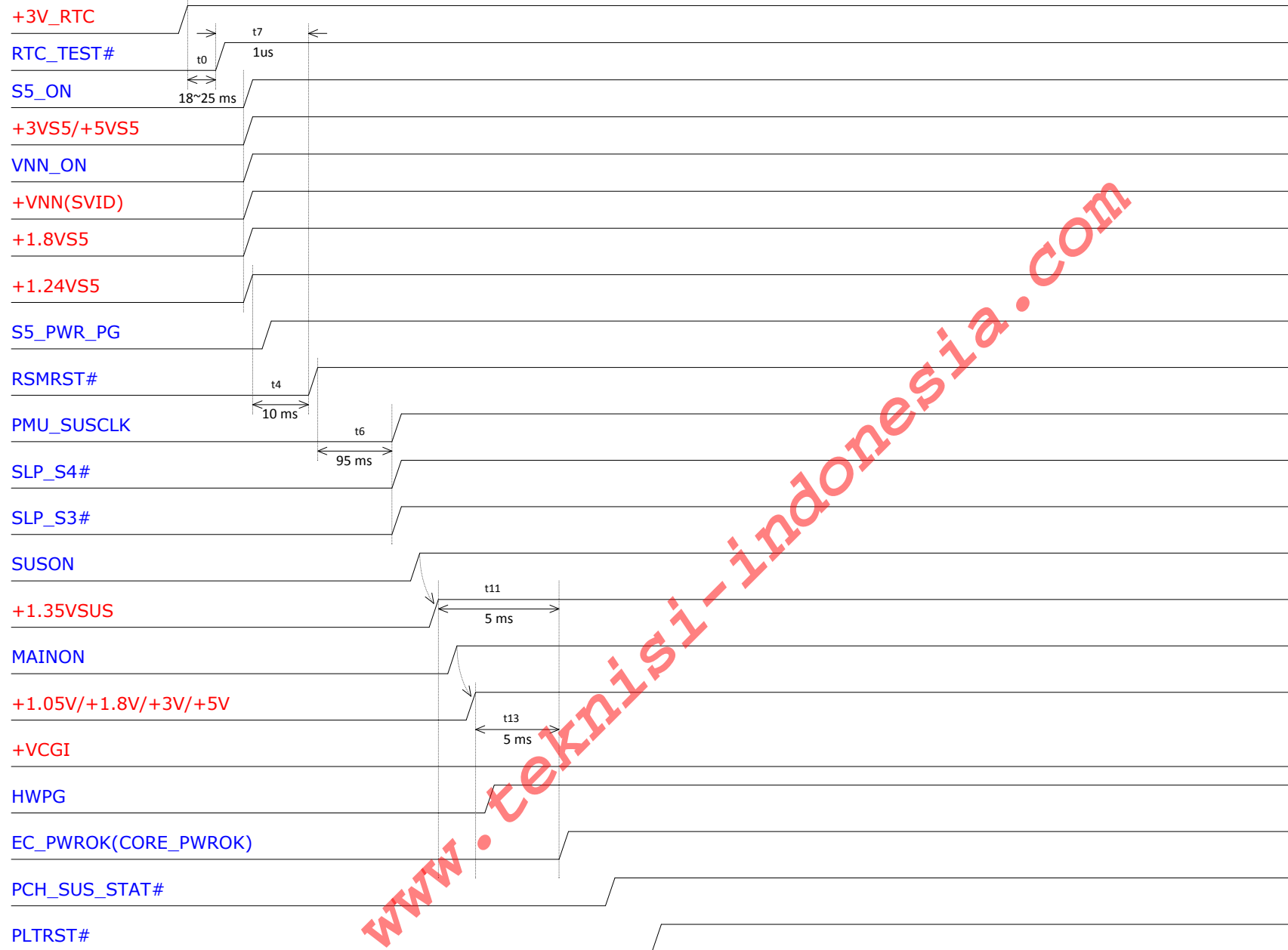
Quanta Computer Inc.

Size	Document Number	Rev
	PTC Circuit	1A
Date:	Thursday, September 08, 2016	Sheet 34 of 40



PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	1A
Date:	Thursday, September 08, 2016	Sheet 35 of 40



PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev.
	Power sequence	1A
Date:	Thursday, September 08, 2016	Sheet 36 of 40

LI8 EE Schematic EC Tracking Record A to B version(SDV/FVT Planar)

EC #	Page	Description	Part Affected
EC-FVT-01	24	Modify LED limited circuit resistor value the same as Newton 1.	R301,R306
EC-FVT-02	13	Buyer request change CAP PN due to EOD issue.	C238
EC-FVT-03	12	Stuff 100K to keep RSMRST# low after S5_ON ramped.	R321
EC-FVT-04	15	Add level shift for TPM reset pin.	Add Q47,R512,R507 Reserve Q46,R245
EC-FVT-05	21	S5_ON PU RES change to 10K to solve can't power on issue.	R468
EC-FVT-06	21	Modify R26/R21 PU power rail to solve can't power on issue.	
EC-FVT-07	12	Add CLKREQ# level shift circuit	Add U34,R510,R511 Reserve R508,R509
EC-FVT-08	3	Modify CLKREQ# PU power rail to +1.8VS5	
EC-FVT-09	15	Modify TPM footprint for pin4/pin11	U14
EC-FVT-10	18	RDC request to modify SSD CONN footprint	CN16
EC-FVT-11	3	Un-stuff BIOS ROM socket	Delete U29,U16 Add U17
EC-FVT-12	10	Un-stuff XDP CONN	Delete CN4
EC-FVT-13	5	Modify BID for FVT stage	Un-stuff R325; Stuff R342
EC-FVT-14	16,24,14	Follow ESD team request to modify ESD component P/N	SC8,SC13 Add EC8
EC-FVT-15	21	Un-stuff ESD component	Delete SC20
EC-FVT-16	6	Intel recommend to un-stuff RSMRST# & CORE_PWROK PU RES	Delete R391,R396
EC-FVT-17	21	Change RES value	R436
EC-FVT-18	5,16	Delete components which is workaround for ES sample CPU	Delete R145,R140,R146
EC-FVT-19	21	Modify EC pin11 VCC power rail to fix 3VPCU can't drop to 0V while press reset button	Add R13 Delete R19



PROJECT : LI8G
Quanta Computer Inc.

[illegible]

LI8G EE Schematic EC Tracking Record B to C version(FVT -> SIT Planar)

EC #	Page	Description	Part Affected
EC-SIT-01	5	Modify KB LED GPIO to fix LED always on issue	
EC-SIT-02	21	Add MOS to turn off S5_ON while press EC reset button	Add Q50,R517
EC-SIT-03	16	Un-stuff Q30 to fix external MIC no function issue	Delete Q30 ; Add R484
EC-SIT-04	22	Modify MOS enable pin to fix press 4s power button shut down can't power on issue	
EC-SIT-05	22	Un-stuff diode and replace it with 0ohm	Delete D19 ; Add R513
EC-SIT-06	22	Modify PU RES value to 10K	R479
EC-SIT-07	22	Modify PTC circuit RES value to 100K	R458
EC-SIT-08	24	Un-stuff power on LED due to light leakage issue	Delete LED2,R284
EC-SIT-09	3	Follow Intel DG to PD USB2_VBUS_SNS	Delete R106 ; Add R113
EC-SIT-10	3	Follow Intel DG to PD USB2_DUALROLE_ID oin and reserve PU RES	Delete R105
EC-SIT-11	24	Modify KB LED limited-current RES value to meet test criteria	R290,R294
EC-SIT-12	21,26	Connect battery enable pin to EC	Delete PR111 ; Add R515
EC-SIT-13	19	WLAN power connect to +3.3V directly	Delete F4 ; Add F10
EC-SIT-14	13,19	Delete diode & PU RES due to no leakage concern	Delete D9,D10,R171,R173 ; Add R518,R519
EC-SIT-15	16	Modify ACZ_BCLK_AUDIO CAP value to fix Jitter over Spec issue	C148
EC-SIT-16	6	Add diode to fix can't power on until plug RTC issue	Add D25
EC-SIT-17	6	Stuff RTC_RST circuit	Add R477,R478
EC-SIT-18	21	Modify power rail to fix S5 leakage issue	Delete R13 ; Add R19
EC-SIT-19	5	Reserve IERR function	Delete R328 ; Add Q27
EC-SIT-20	13	Delete MOS which is no used for LCD_BK_OFF function	Delete Q6
EC-SIT-21	6	Modify TP to larger one	TP17,TP21
EC-SIT-22	16	Modify RES value to fix BIOS beep no sound issue	R250
EC-SIT-23	21	Connect THRMTRIP# to EC GPIO pin directly(reserve)	
EC-SIT-24	21	Reserve test point	Add TP56,TP57,TP58
EC-SIT-25	5	Modify board ID for SIT stage	Delete R324,R342 ; Add R341,R325
EC-SIT-26	20	Change USB power switch PN to 1.5A	U27,U28
EC-SIT-27	13	PN EOD issue	C238
EC-SIT-28	24	Modify PN	R301
EC-SIT-29	20	PN EOD issue	R184



PROJECT : LI8G
Quanta Computer Inc.

LI8G Power Schematic EC Tracking Record B to C version(FVT -> SIT Planar)

40

EC #	Page	Description	Part Affected
EC-SIT-P01	33	Remove +3VSUS net which is no used	
EC-SIT-P02	29	Change source	PR178,PR135,PR152
www.teknisi-indonesia.com			